



# BCP240T

## HIGH EFFICIENCY HETEROJUNCTION POWER FET CHIP (.25μm x 2400μm)

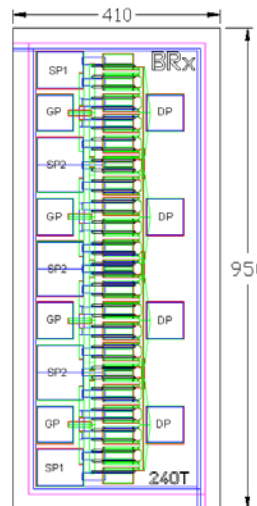
The BeRex BCP240T is a GaAs Power pHEMT with a nominal 0.25 micron gate length and 2400 micron gate width making the product ideally suited for amplifier applications where high-gain and medium power from DC to 26 GHz. The product may be used in either wideband or narrow-band applications. The BCP240T is produced using state of the art metallization with Si<sub>3</sub>N<sub>4</sub> passivation and is screened to assure reliability.

### PRODUCT FEATURES

- 34 dBm Typical Output Power
- 10 dB Typical Gain @12 GHz
- 58% PAE Typical @12 GHz
- 0.25 X 2400 μm Recessed Gate

### APPLICATIONS

- Commercial
- Military / Hi-Rel.
- Test & Measurement



Chip dimensions : 410 X 950 microns  
 Gate pad(GP) : 75 X 75 microns  
 Drain pad(DP) : 75 X 75 microns  
 Source pad1(SP1) : 95 X 75 microns  
 Source pad2(SP2) : 95 X 110 microns  
 Chip thickness : 100 microns

### DC CHARACTERISTICS T<sub>a</sub> = 25° C

SYMBOL	PARAMETER/TEST CONDITIONS	MIN.	TYPICAL	MAX.	UNIT
I <sub>dss</sub>	Saturated Drain Current (V <sub>gs</sub> = 0V, V <sub>ds</sub> = 1.2V)	480	720	960	mA
G <sub>m</sub>	Transconductance (V <sub>ds</sub> = 2V, V <sub>gs</sub> = 50% I <sub>dss</sub> )		960		mS
V <sub>p</sub>	Pinch-off Voltage (I <sub>ds</sub> = 2.4 mA, V <sub>ds</sub> = 2V)	-2.5	-1.1	-0.5	V
BV <sub>gd</sub>	Drain Breakdown Voltage (I <sub>g</sub> = 2.4 mA, source open)		-15	-12	V
BV <sub>gs</sub>	Source Breakdown Voltage (I <sub>g</sub> = 2.4 mA, drain open)		-13		V
R <sub>th</sub>	Thermal Resistance (Au-Sn Eutectic Attach)		23		° C/W

### ELECTRICAL CHARACTERISTICS (TUNED FOR POWER) T<sub>a</sub> = 25° C

SYMBOL	PARAMETER/TEST CONDITIONS	TEST FREQ.	MIN.	TYPICAL	MAX.	UNIT
P <sub>1dB</sub>	Output Power @ P <sub>1dB</sub> (V <sub>ds</sub> = 8V, I <sub>ds</sub> = 50% I <sub>dss</sub> )	12 GHz 18 GHz	33.5	34.8 33.7		dBm
G <sub>1dB</sub>	Gain @ P <sub>1dB</sub> (V <sub>ds</sub> = 8V, I <sub>ds</sub> = 50% I <sub>dss</sub> )	12 GHz 18 GHz	9.0	10.2 7.7		dB
PAE	PAE @ P <sub>1dB</sub> (V <sub>ds</sub> = 8V, I <sub>ds</sub> = 50% I <sub>dss</sub> )	12 GHz 18 GHz		58 42		%

ELECTRICAL CHARACTERISTICS (TUNED FOR GAIN)  $T_a = 25^\circ\text{C}$

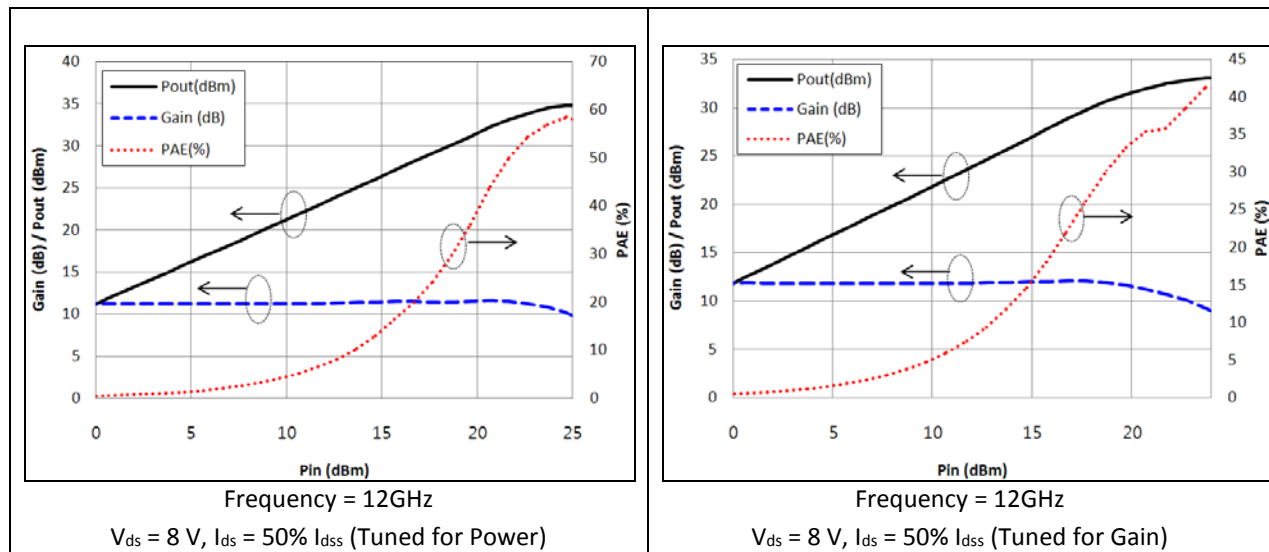
SYMBOL	PARAMETER/TEST CONDITIONS	TEST FREQ.	MIN.	TYPICAL	MAX.	UNIT
$P_{1dB}$	Output Power @ $P_{1dB}$ ( $V_{ds} = 8\text{V}$ , $I_{ds} = 50\% I_{dss}$ )	12 GHz 18 GHz	31.0	32.5 31.2		dBm
$G_{1dB}$	Gain @ $P_{1dB}$ ( $V_{ds} = 8\text{V}$ , $I_{ds} = 50\% I_{dss}$ )	12 GHz 18 GHz	9.5	11.0 8.7		dB
PAE	PAE @ $P_{1dB}$ ( $V_{ds} = 8\text{V}$ , $I_{ds} = 50\% I_{dss}$ )	12 GHz 18 GHz		36 27		%

MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

SYMBOLS	PARAMETERS	ABSOLUTE	CONTINUOUS
$V_{ds}$	Drain-Source Voltage	12 V	8 V
$V_{gs}$	Gate-Source Voltage	-6 V	-3 V
$I_{ds}$	Drain Current	$I_{dss}$	690 mA
$I_{gsf}$	Forward Gate Current	120 mA	20 mA
$P_{in}$	Input Power	31 dBm	@ 3dB Compression
$T_{ch}$	Channel Temperature	175° C	150° C
$T_{stg}$	Storage Temperature	-60° C - 150° C	-60° C - 150° C
$P_t$	Total Power Dissipation	8.4 W	6.9 W

Exceeding any of the above Maximum Ratings will result in reduced MTTF and may cause permanent damage to the device.

$P_{IN\_P_{OUT}}$ /Gain, PAE (12 GHz)



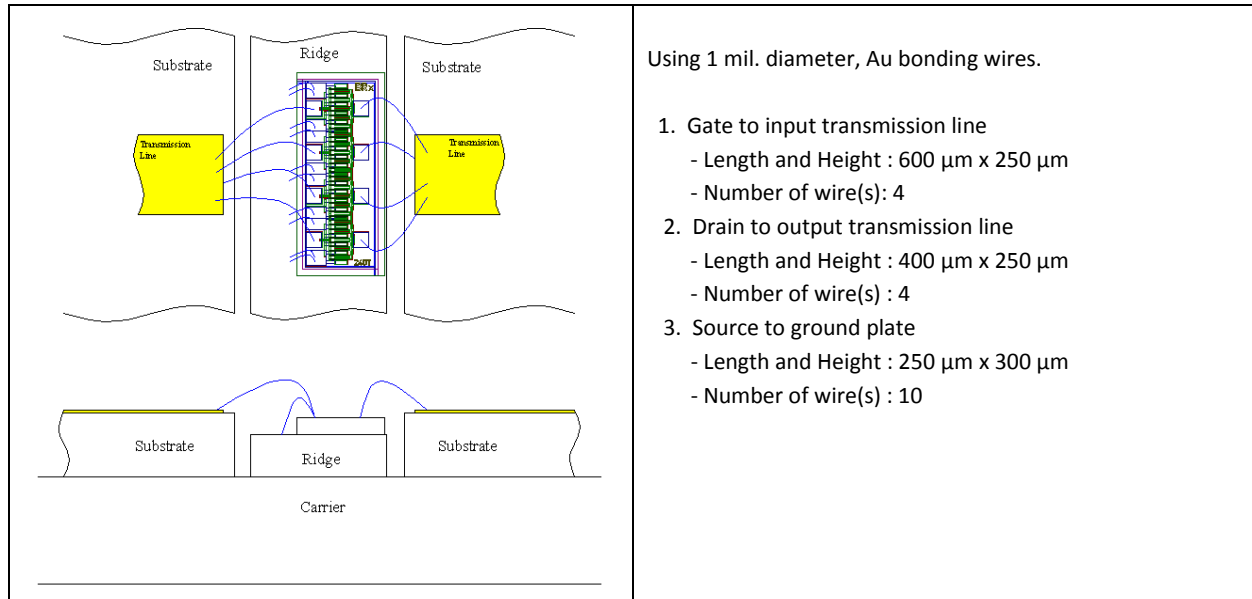
S-PARAMETER ( $V_{ds} = 8V$ ,  $I_{ds} = 50\% I_{dss}$ )

FREQ. [GHZ]	S11 [MAG]	S11 [ANG.]	S21 [MAG]	S21 [ANG.]	S12 [MAG]	S12 [ANG.]	S22 [MAG]	S22 [ANG.]
1	0.90	-147.20	10.68	101.84	0.024	26.83	0.54	-166.95
2	0.90	-166.80	5.52	87.86	0.026	31.25	0.56	-173.49
3	0.91	-175.23	3.72	79.48	0.028	32.71	0.57	-175.76
4	0.92	179.32	2.80	72.74	0.032	38.68	0.58	-176.62
5	0.92	175.65	2.22	66.25	0.033	42.56	0.59	-177.49
6	0.92	172.96	1.84	60.88	0.037	47.19	0.60	-178.08
7	0.92	170.17	1.54	55.39	0.039	49.21	0.61	-178.49
8	0.93	167.87	1.35	50.23	0.040	52.94	0.62	-178.60
9	0.93	165.98	1.21	46.31	0.045	50.65	0.63	-179.68
10	0.92	163.50	1.09	41.28	0.048	53.68	0.64	179.89
11	0.93	161.40	0.99	36.84	0.052	54.32	0.65	179.02
12	0.93	158.76	0.91	32.10	0.054	53.07	0.66	178.15
13	0.93	154.63	0.85	27.43	0.056	53.42	0.67	177.02
14	0.94	151.80	0.78	22.74	0.058	51.40	0.68	175.57
15	0.93	148.54	0.72	17.87	0.061	50.66	0.69	173.37
16	0.94	143.75	0.67	12.61	0.062	47.94	0.71	171.14
17	0.94	140.71	0.62	7.15	0.063	44.66	0.72	168.48
18	0.94	136.72	0.56	2.33	0.065	40.30	0.74	166.01
19	0.95	132.10	0.51	-3.25	0.064	41.04	0.76	163.20
20	0.96	131.00	0.46	-7.07	0.063	37.85	0.77	161.05
21	0.96	128.78	0.41	-10.67	0.064	35.99	0.78	158.85
22	0.96	126.73	0.37	-13.78	0.063	35.56	0.79	157.27
23	0.95	127.90	0.33	-15.97	0.064	32.67	0.80	154.94
24	0.95	126.96	0.30	-17.87	0.064	27.92	0.82	154.34
25	0.96	127.60	0.27	-19.52	0.061	28.05	0.82	153.29
26	0.95	130.57	0.25	-18.60	0.058	37.30	0.83	153.31

Note: S-parameters include bond wires. Reference planes are at edge of substrates shown on "Wire Bonding Information" figure below.

## WIRE BONDING INFORMATION

Follow the wire bonding diagrams recommended by BeRex below to achieve optimum device performance. BeRex recommends thermo-compression wedge bonding. As a general rule, bonding temperature should be kept to a maximum of 280°C for no longer than 2 minutes for all bonding wires. Ultrasonic bonding is not recommended.



Proper ESD procedures should be followed when handling this device.

### DIE ATTACH RECOMMENDATIONS:

BeRex recommends the “Eutectic” die attach using Au-Sn (80%-20%) pre-forms. The die attach station must have accurate temperature control, and the operation should be performed with parts no hotter than 300°C for less than 10 seconds. An inert forming gas (90% N<sub>2</sub>-10% H<sub>2</sub>) or clean, dry N<sub>2</sub> should be used.

### HANDLING PRECAUTIONS:

GaAs FETs are very sensitive to and may be damaged by Electrostatic Discharge (ESD). Therefore, proper ESD precautions must be taken whenever you are handling these devices. It is critically important that all work surfaces, and assembly equipment, as well as the operator be properly grounded when handling these devices to prevent ESD damage.

### STORAGE & SHIPPING:

BeRex’s standard chip device shipping package consists of an antistatic “Gel-Pak”, holding the chips, placed inside a sealed antistatic and moisture barrier bag. This packaging is designed to provide a reasonable measure of protection from both mechanical and ESD damage.

Chip devices should be stored in a clean, dry Nitrogen gas environment at room temperature until they are required for assembly. Only open the shipping package or perform die assembly in a work area with a class 10,000 or better clean room environment to prevent contamination of the exposed devices.

**CAUTION:**

THIS PRODUCT CONTAINS GALLIUM ARSENIDE (GaAs) WHICH CAN BE HAZARDOUS TO THE HUMAN BODY AND THE ENVIRONMENT. THEREFORE, IT MUST BE HANDLED WITH CARE AND IN ACCORDANCE WITH ALL GOVERNMENTAL AND COMPANY REGULATIONS FOR THE SAFE HANDLING AND DISPOSAL OF HAZARDOUS WASTE. DO NOT BURN, DESTROY, CUT, CRUSH OR CHEMICALLY DISSOLVE THE PRODUCT. DO NOT LICK THE PRODUCT OR IN ANY WAY ALLOW IT TO ENTER THE MOUTH. EXCLUDE THE PRODUCT FROM GENERAL INDUSTRIAL WASTE OR GARBAGE AND DISPOSE OF ONLY IN ACCORDANCE TO APPLICABLE LAWS AND/OR ORDINANCES.

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**RoHS COMPLIANT**

For complete specifications, S-parameters and information on bonding and handling, visited our website; [www.berex.com](http://www.berex.com)