BDA4601

6-bit Digital Step Attenuator

1MHz– 4000MHz

Device Features

- 6-bit Serial & Parallel Interface
- 31.5 dB Control Range 0.5 dB step
- No positive glitch
- 2.7 V to 5.5 V supply
- 1.8 V or 3.3 V control logic
- Any bit Attenuation Error < ±0.6 dB up to 3GHz
- Low Insertion Loss
  - 0.7dB @ 1MHz
  - 1.0 dB @ 1GHz
  - 1.3 dB @ 2GHz
  - 1.7 dB @ 3GHz
  - 2.6 dB @ 4GHz
- High linearity IIP3 > +55 dBm
- Input 0.1dB Compression (P0.1dB) 31dBm
- Programming modes
  - Direct parallel
  - Latched parallel
  - Serial
- Support function power up state selection with PUP1,2 pin
- Stable Integral Non-Linearity over temperature
- Low Current Consumption 150 µA typical
- -40 °C to +105 °C operating temperature
- ESD rating : Class2 (2KV HBM)
- Lead-free/RoHS-compliant 20-lead 4x4mm QFN SMT package

20-lead 4mm x 4 mm x 0.9mm QFN

Figure 1. Package Type

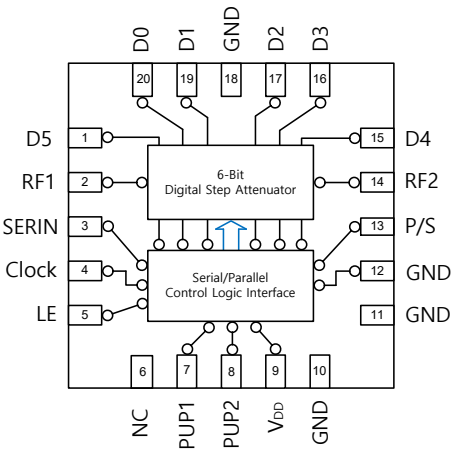


Figure 2. Functional Block Diagram

Product Description

The BDA4601 is a 50Ω digital step attenuator model which provides adjustable attenuation from 0 to 31.5 dB in 0.5 dB steps. The control is a 6-bit serial interface and parallel interface.

BDA4601 supports a broad operating frequency range from 1MHz to 4.0 GHz. BDA4601 is offering the High linearity, low power consumption, low insertion loss and high attenuation accuracy.

The device features safe state transitions with No positive Glitch technology. and is optimized for excellent step accuracy

The RF input and output are internally matched to 50 Ω and do not require any external matching components. The design is bidirectional; therefore, the RF input and output are interchangeable.

This DSA does not require blocking capacitors. If DC is presented at the RF port, add a blocking capacitor.
It is packaged in a RoHS-compliant with QFN surface mount package.

Application

- Cellular Base station/Repeater Infrastructure
- Digital Pre-Distortion
- Point to Point
- Test Equipment and sensors
- Military Wireless system
- Cable Infrastructure
- General purpose Wireless

Table 1. Electrical Specifications[1]

Parameter		Condition		Frequency	Min	Typ	Max	Unit
Operational Frequency Range					1		4000	MHz
Insertion Loss[2]		Attenuation (ATT) = 0dB		1GHz		1		dB
				2GHz		1.3		dB
				3GHz		1.7		dB
				4GHz		2.6		dB
Attenuation	**Range**	0.5dB step				0 - 31.5		dB
	Accuracy	Any bit or bit combination		1MHz - 1GHz	±(0.15 + 1% of attenuation state)			dB
				> 1 - 2.2GHz	±(0.15 + 2% of attenuation state)			
				> 2.2 - 3GHz	±(0.15 + 5% of attenuation state)			
				> 3 - 4GHz	±(0.15 + 6% of attenuation state)			
Return loss	**Input Return Loss**	ATT= 0dB		1 - 2GHz		18		dB
				> 2 - 4GHz		13		
	Output Return Loss			1 - 2GHz		17		
				> 2 - 4GHz		13		
Relative Phase		ATT = 0dB		1GHz		10		degree
				2GHz		20		
				3GHz		32		
				4GHz		40		
Input Linearity	**Input 0.1dB Compression**	ATT = 0dB		1.95GHz		31		dBm
				3.5GHz		31		dBm
	Input IP3	Pin = +15dBm/tone Δf = 10KHz	ATT = 0.0dB RFin = RF1	1.95GHz		61		dBm
			ATT = 0.0dB RFin = RF2			57		
			ATT= 15.5dB RFin = RF1			59		
			ATT = 15.5dB RFin = RF2			57		
		Pin = +15dBm/tone Δf = 10KHz	ATT = 0.0dB RFin = RF1	3.5GHz		59		dBm
			ATT = 0.0dB RFin = RF2			60		
			ATT = 15.5dB RFin = RF1			63		
			ATT = 15.5dB RFin = RF2			61		
Switching Time		50% CTRL to 90% or 10% RF				500	800	ns
Maximum Spurious Level		Measured at DSA RF1,RF2 ports		1 - 50MHz		-123		dBm/10Hz
				50 - 200MHz		-135		
				>200MHz[3]		< -145		

1. Device performance _ measured on a BeRex Evaluation board Kit at 25°C, 50 Ω system, VDD=+3.3V
2. All data has PCB insertion loss de-embedded.
3. No spurious signals were detected above 200MHz.

Table 2. Recommended operating Condition

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Supply Voltages		V_{DD}		2.7		5.5	V
Supply Current		I_{DD}			150	360	μA
Digital Control Input	High	V_{CTLH}	V_{DD}=3.3V or 5V	1.17		3.6	V
	Low	V_{CTLL}	V_{DD}=3.3V or 5V	-0.3		0.6	V
Operating Temperature Range		T_{case}	Exposed Paddle	-40		105	˚C
RF Max Input Power		P_{IN_CW}	RF1 or RF2, CW			23	dBm
Impedance		Z_{Load}	Single ended		50		Ω

Specifications are not guaranteed over all recommended operating conditions.

Table 3. Absolute Maximum Ratings

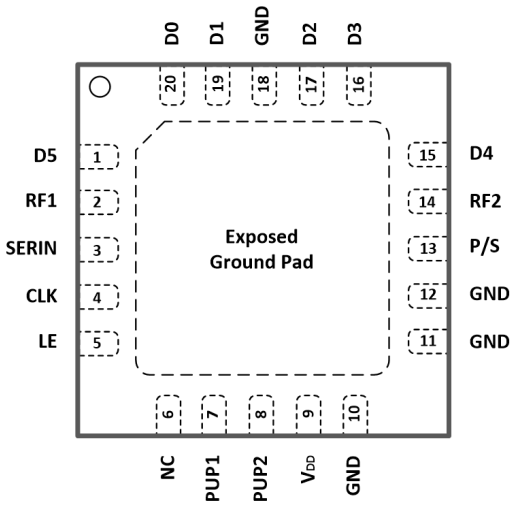
Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{DD}	-0.3		5.5	V
Digital input voltage		V_{CTL}	-0.3		3.6	V
Maximum input power		P_{IN_CWMAX}			31	dBm
Temperature	Junction	T_J			140	℃
	Storage	T_{ST}	-65		150	℃
	Reflow	T_R			260	℃
ESD Sensitivity	HBM[1]	ESD_{HBM}			±2000 (Class 2)	V
	CDM[2]	ESD_{CDM}			±500 (Class C2)	V

Operation of this device above any of these parameters may result in permanent damage.
1. HBM : Human Body Model (JEDEC **JS-001-2017**)
2. CDM : Charged Device Model (JEDEC **JESD22-C101F**)

Table 4. Package Thermal Characteristics

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	37.4	˚C/W

Figure 3. Pin Configuration (Top View)



* Device is RF Bi -Directional

Table 5. Pin Descriptions

Pin	Pin name	Description
1	D5	Parallel Control Voltage Inputs, Attenuation control bit 16dB
2	RF1[1]	RF1 port (Attenuator RF Input) This pin can also be used as an output because the design is bidirectional. RF1 is dc-coupled and matched to 50 Ω
3	SERIN	Serial interface data input
4	CLK	Serial interface clock input
5	LE	Latch Enable input. This pin is recommended to pull-down.
6	NC	Not Connected
7	PUP1	Power-Up State Selection Bits. These pins set the attenuation value at power-up (see Table 12). There is no internal pull-up or pull-down resistor on these pins; therefore, they must always be kept at a valid logic level (V_{CTLH} or V_{CTLL}) and not be left floating
8	PUP2	
9	V_{DD}	Supply voltage (nominal 3.3V)
13	P/S	Parallel/Serial Mode Select. For parallel mode operation, set this pin to LOW. For serial mode operation, set this pin to HIGH.
14	RF2[1]	RF2 port (Attenuator RF Output.) This pin can also be used as an input because the design is bidirectional. RF2 is dc-coupled and matched to 50 Ω.
15	D4	Parallel Control Voltage Inputs, Attenuation control bit 8dB
16	D3	Parallel Control Voltage Inputs, Attenuation control bit 4dB
17	D2	Parallel Control Voltage Inputs, Attenuation control bit 2dB
19	D1	Parallel Control Voltage Inputs, Attenuation control bit 1dB
20	D0	Parallel Control Voltage Inputs, Attenuation control bit 0.5dB
Pad	GND	Exposed pad: The exposed pad must be connected to ground for proper operation
10,11,12,18	GND	Ground, These pins must be connected to ground

1. RF pins 2 and 14 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met

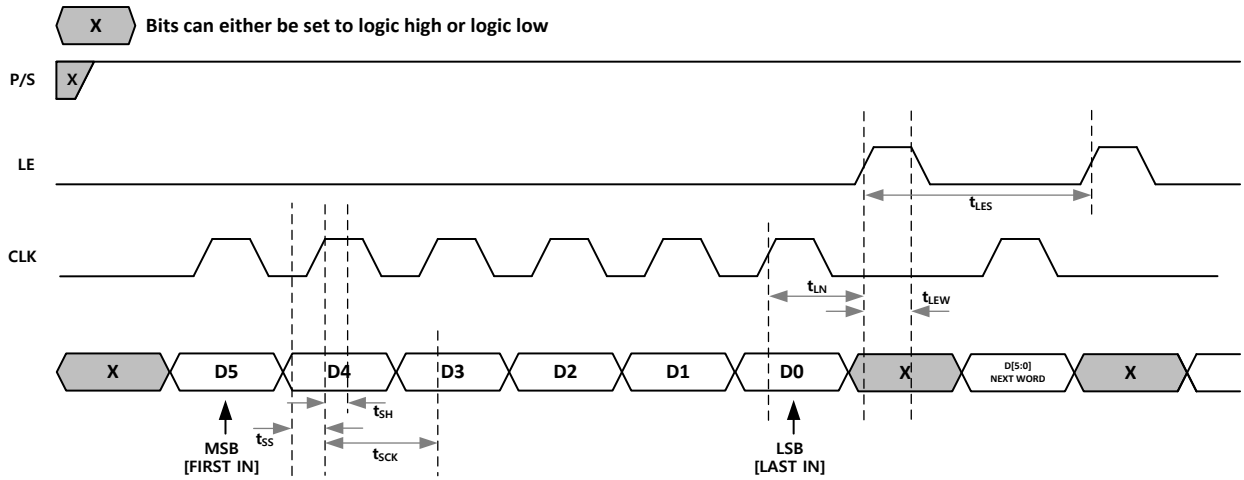
Programming Options

BDA4601 can be programmed using either the parallel or serial interface, which is selectable via P/S pin(Pin13).
Serial mode is selected by pulling it to a voltage logic HIGH and parallel mode is selected by setting P/S to logic LOW

Serial Control Mode

The serial interface is a 6 bit shift register to shift in the data MSB (D5) first. When serial programming is used, It is recommended all the parallel control input pins (1, 15, 16, 17, 19, 20) are grounded.
It is controlled by three CMOS-compatible signals: SERIN, Clock, and Latch Enable (LE).

Figure 4. Serial Mode Timing Diagram



The BDA4601 has a 3-wire serial peripheral interface (SPI): serial data input (SERIN), clock (CLK), and latch enable (LE). The serial control interface is activated when P/S is set to HIGH.

In serial mode, the 6-bit Data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggled HIGH to latch the new attenuation state into the device. LE must be set to LOW to clock new 6-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept HIGH (see Figure 4 and Table 7).

Table 6. 6-bit Serial Word Sequence

D5	Attenuation 16dB Control Bit
D4	Attenuation 8dB Control Bit
D3	Attenuation 4dB Control Bit
D2	Attenuation 2dB Control Bit
D1	Attenuation 1dB Control Bit
D0	Attenuation 0.5dB Control Bit

Table 7. Truth Table for Serial Control Word

Digital Control Input						Attenuation state (dB)
D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	
LOW	LOW	LOW	LOW	LOW	LOW	0 (RL)
LOW	LOW	LOW	LOW	LOW	HIGH	0.5
LOW	LOW	LOW	LOW	HIGH	LOW	1
LOW	LOW	LOW	HIGH	LOW	LOW	2
LOW	LOW	HIGH	LOW	LOW	LOW	4
LOW	HIGH	LOW	LOW	LOW	LOW	8
HIGH	LOW	LOW	LOW	LOW	LOW	16
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	31.5

Table 8. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{Clk}	Serial data clock frequency			10	MHz
t_{SCK}	Minimum serial period	70			
t_{SS}	Serial Data setup time	10			
t_{SH}	Serial Data hold time	10			
t_{LN}	LE setup time	10			
t_{LEW}	Minimum LE pulse width	30			
t_{LES}	Minimum LE pulse spacing		600		

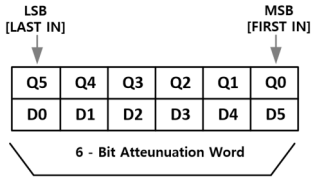
Table 9. Mode Selection

P/S	Control Mode
LOW	Parallel
HIGH	Serial

Serial Register Map

The BDA4601 can be programmed via the serial control on the rising edge of Latch Enable (LE) which loads the last 6-bits data word in the SHIFT Register. Serial data is clocked in MSB(D5) first.

Figure 5. Serial Register Map



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four, then convert to binary.
For example, to program the 15.5dB state :

2 x 15.5 = 31
D0—D5 : 111110

Serial Input : 111110

1	1	1	1	1	0
D0	D1	D2	D3	D4	D5

Parallel Control Mode

The BDA4601 has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 10. The parallel control interface is activated when P/S is set to LOW. There are two modes of parallel operation: direct parallel and latched parallel

Direct Parallel Mode

The LE pin must be kept HIGH. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 1, 15, 16, 17,19, 20]. Use direct parallel mode for the fastest settling time.

Latched Parallel Mode

The LE pin must be kept LOW when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled HIGH to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled LOW to latch the change into the device until the next desired attenuation change (see Figure 5 and Table 10).

Figure 5. Latched Parallel Mode Timing Diagram

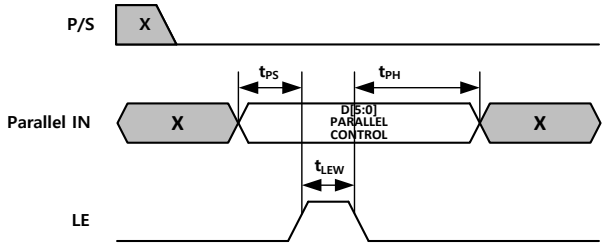


Table 10. Truth Table for the Parallel Control Word

D0	D1	D2	D3	D4	D5	P/S	LE	Attenuation State
LOW	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	Reference Loss
HIGH	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	0.5dB
LOW	HIGH	LOW	LOW	LOW	LOW	LOW	HIGH	1dB
LOW	LOW	HIGH	LOW	LOW	LOW	LOW	HIGH	2dB
LOW	LOW	LOW	HIGH	LOW	LOW	LOW	HIGH	4dB
LOW	LOW	LOW	LOW	HIGH	LOW	LOW	HIGH	8dB
LOW	LOW	LOW	LOW	LOW	HIGH	LOW	HIGH	16dB
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	31.5dB

Table 11. Parallel Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_{LEW}	Minimum LE pulse width	10			ns
t_{PH}	Data hold time from LE	10			ns
t_{PS}	Data setup time to LE	10			ns

Power-UP Interface

The BDA4601 uses the PUP1 and PUP2 control voltage inputs to set the attenuation value to a known value at power-up before the initial control data word is provided in parallel mode.

Power-up Control for Parallel Mode (P/S=LOW)

When the attenuator powers up with LE set to LOW, the state of PUP1 and PUP2 determines the power-up state of the device per the truth table shown in Table 12.

Power-up Control for Serial Mode (P/S=HIGH)

When the attenuator powers up in Serial mode, the six digital control inputs are set to whatever data is present on the six parallel data inputs (D0 to D5, Refer to Table 13). This allows any one of the 64 attenuation settings to be specified as the power-up state.

Table 12. PUP Truth Table for Parallel Control Mode

Attenuation state	P/S	LE	PUP1	PUP2
31.5 dB	LOW	LOW	HIGH	HIGH
16 dB	LOW	LOW	HIGH	LOW
8 dB	LOW	LOW	LOW	HIGH
Reference Loss	LOW	LOW	LOW	LOW
Defined by C0.5-C16	LOW	HIGH	Don't Care	Don't Care

Table 13. PUP Truth Table for Serial Control Mode

Attenuation State	P/S	D0	D1	D2	D3	D4	D5
Reference Loss	HIGH	LOW	LOW	LOW	LOW	LOW	LOW
0.5dB	HIGH	HIGH	LOW	LOW	LOW	LOW	LOW
1dB	HIGH	LOW	HIGH	LOW	LOW	LOW	LOW
2dB	HIGH	LOW	LOW	HIGH	LOW	LOW	LOW
4dB	HIGH	LOW	LOW	LOW	HIGH	LOW	LOW
8dB	HIGH	LOW	LOW	LOW	LOW	HIGH	LOW
16dB	HIGH	LOW	LOW	LOW	LOW	LOW	HIGH
20dB	HIGH	LOW	LOW	LOW	HIGH	LOW	HIGH
24dB	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH
31.5dB	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH

Typical RF Performance Plot - BDA4601 EVK - PCB

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit Rev.2 RF connector and board losses are de-embedded, unless otherwise noted

Figure 6. Insertion loss vs Temperature

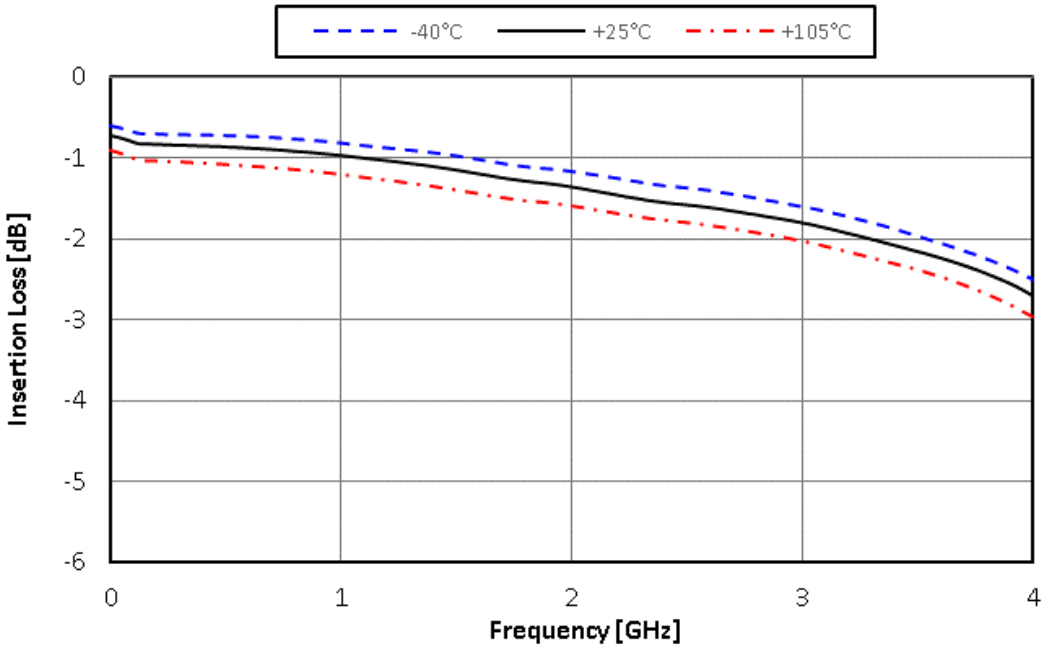
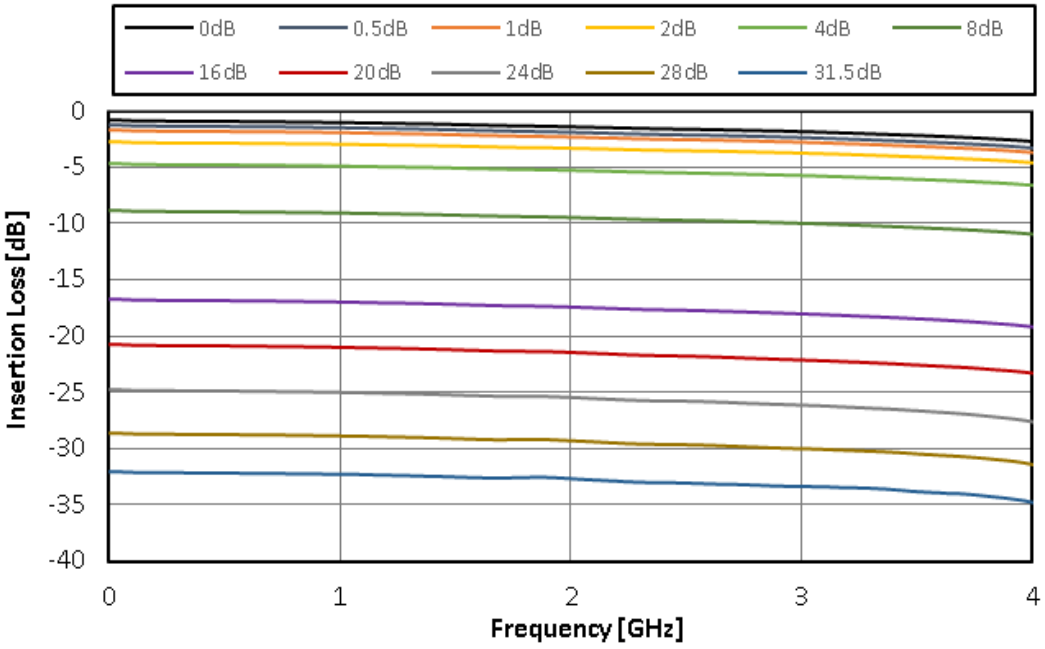


Figure 7. Insertion loss vs Attenuation Setting



Typical RF Performance Plot - BDA4601 EVK - PCB

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit Rev.2 RF connector and board losses are de-embedded, unless otherwise noted

Figure 8. Input Return Loss vs Attenuation Setting

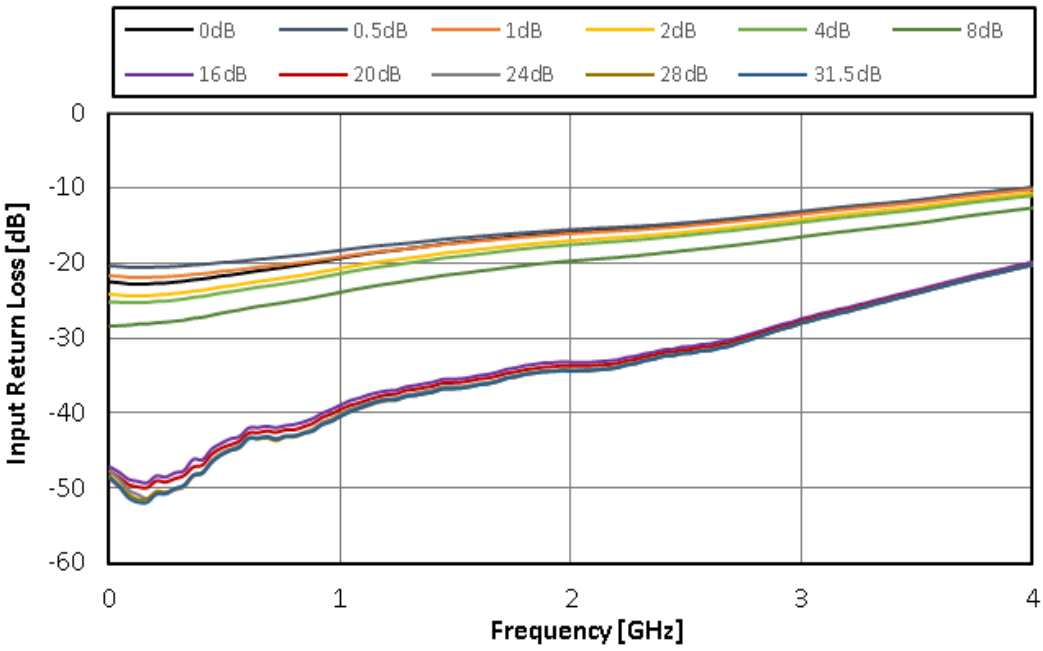
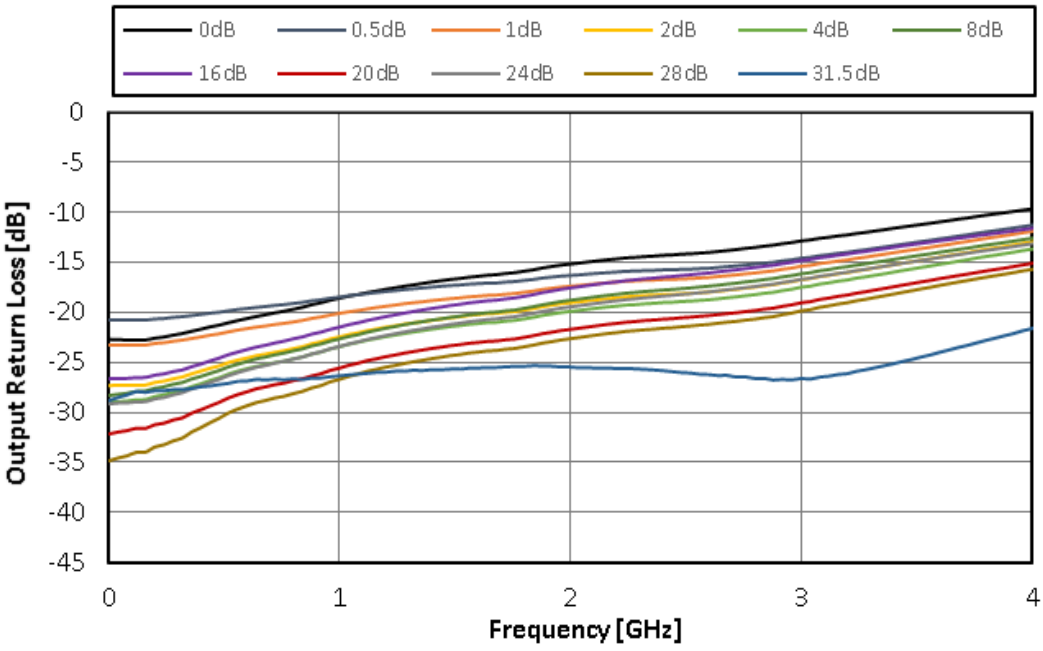


Figure 9. Output Return Loss vs Attenuation Setting



Typical RF Performance Plot - BDA4601 EVK - PCB

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit Rev.2 RF connector and board losses are de-embedded, unless otherwise noted

Figure 10. Input Return Loss for 16dB Attenuation Setting vs Temperature

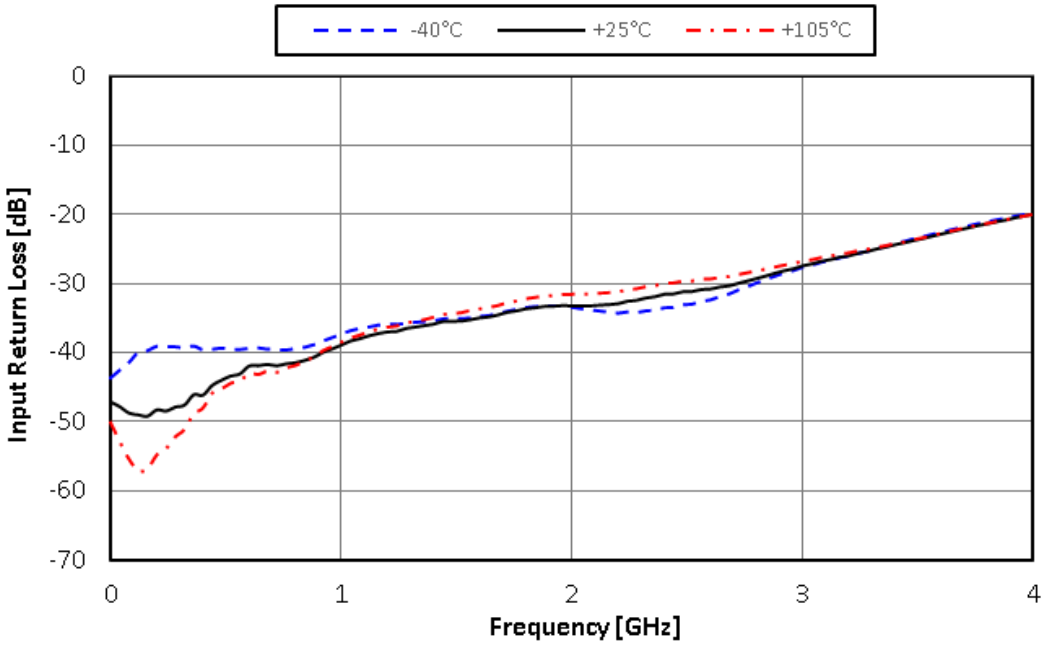
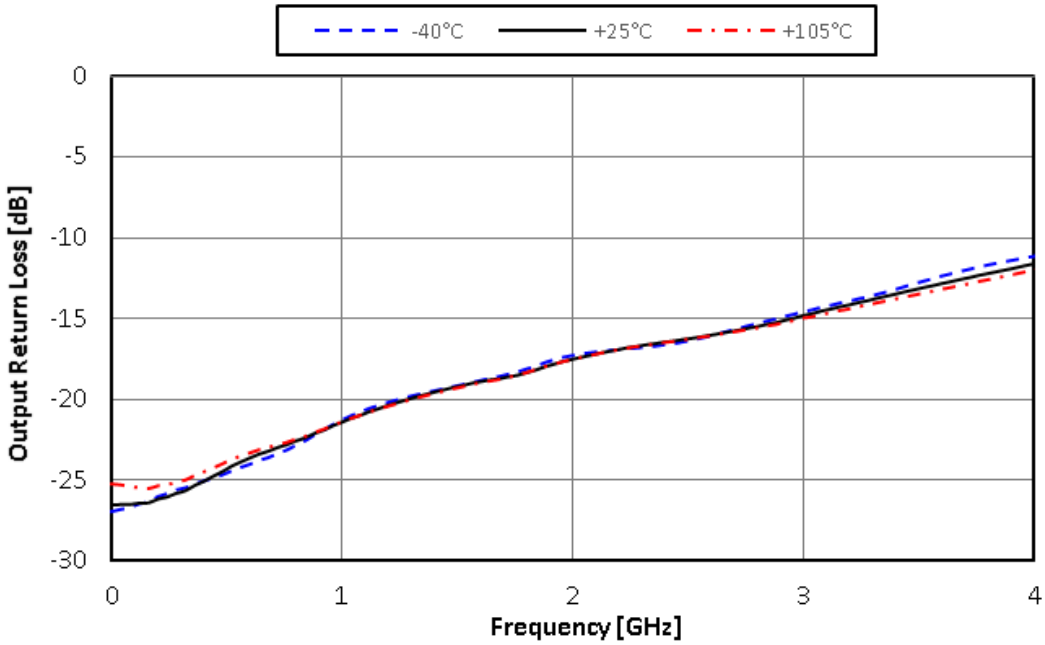


Figure 11. Output Return Loss for 16dB Attenuation Setting vs Temperature



Typical RF Performance Plot - BDA4601 EVK - PCB

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit Rev.2 RF connector and board losses are de-embedded, unless otherwise noted

Figure 12. Relative Phase Error vs Attenuation Setting

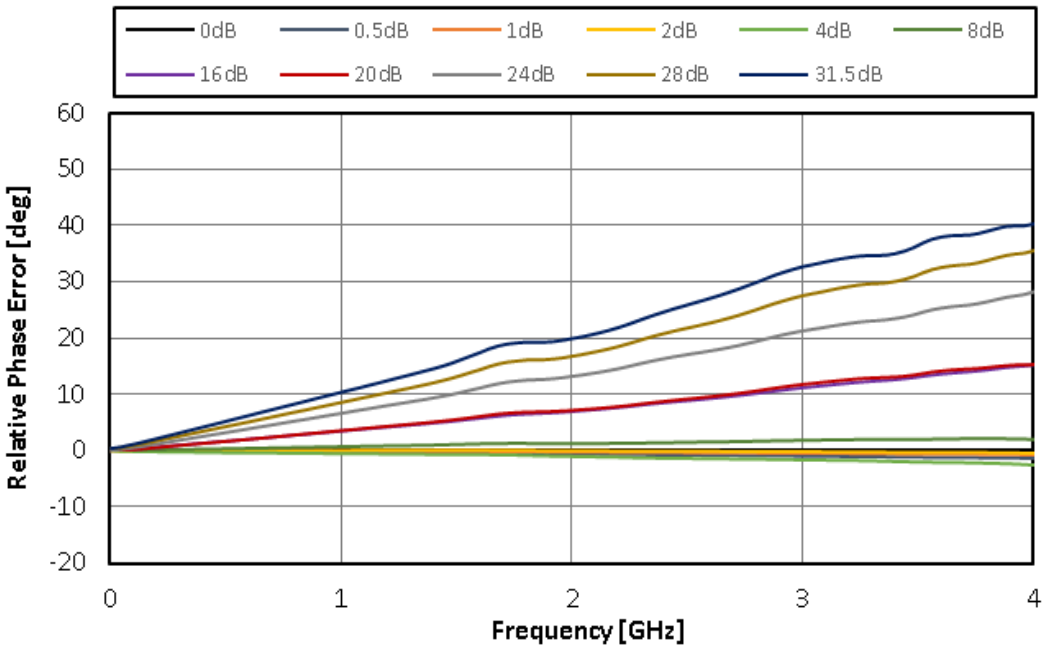
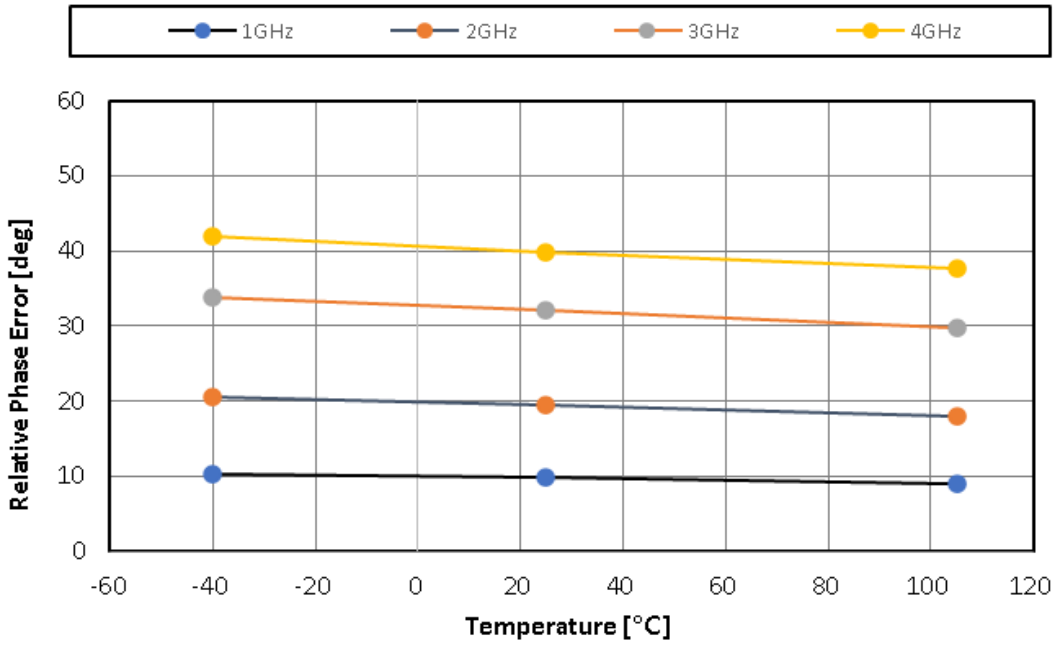


Figure 13. Relative Phase Error for 31.5dB Attenuation Setting vs Frequency



Typical RF Performance Plot - BDA4601 EVK - PCB

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit Rev.2 RF connector and board losses are de-embedded, unless otherwise noted

Figure 14. Attenuation Error @900MHz vs Temperature

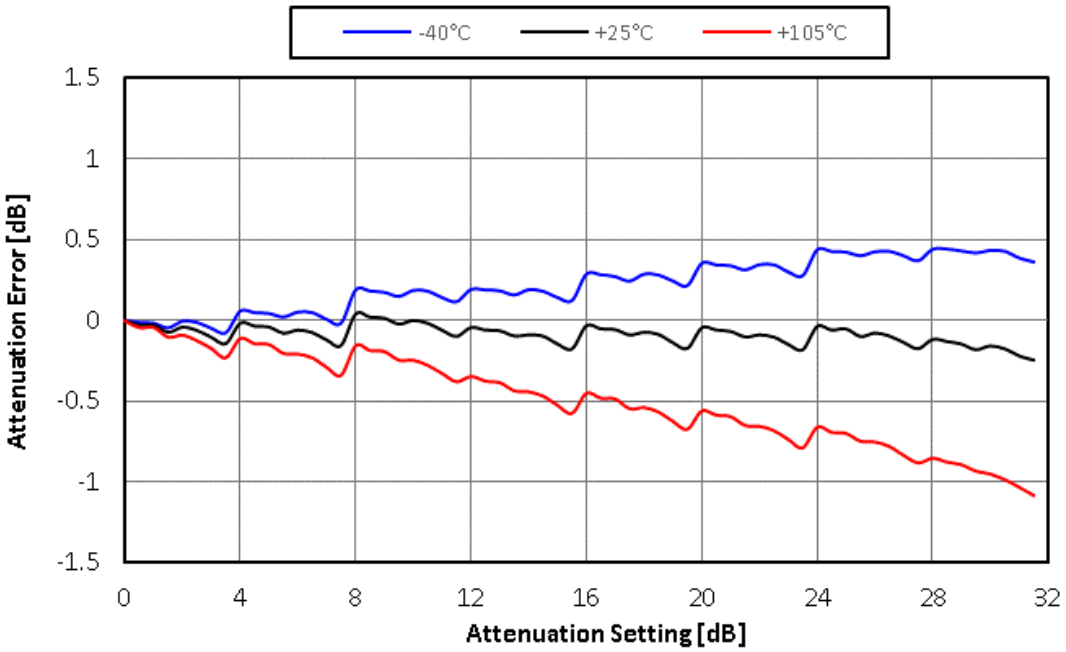
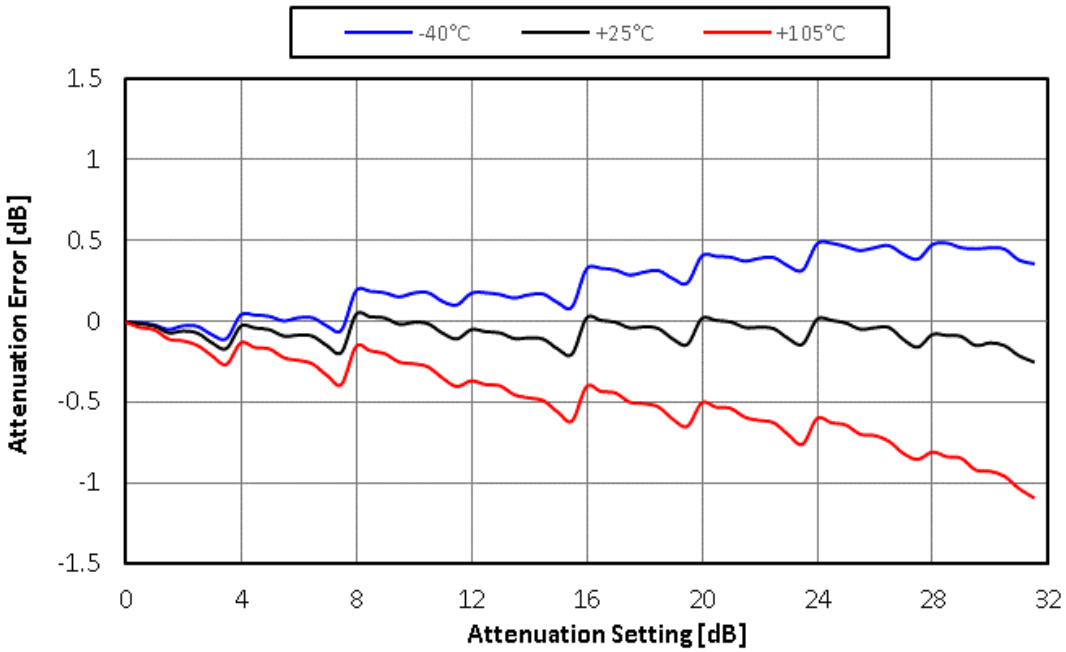


Figure 15. Attenuation Error @1800MHz vs Temperature



Typical RF Performance Plot - BDA4601 EVK - PCB

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit Rev.2 RF connector and board losses are de-embedded, unless otherwise noted

Figure 16. Attenuation Error @2200MHz vs Temperature

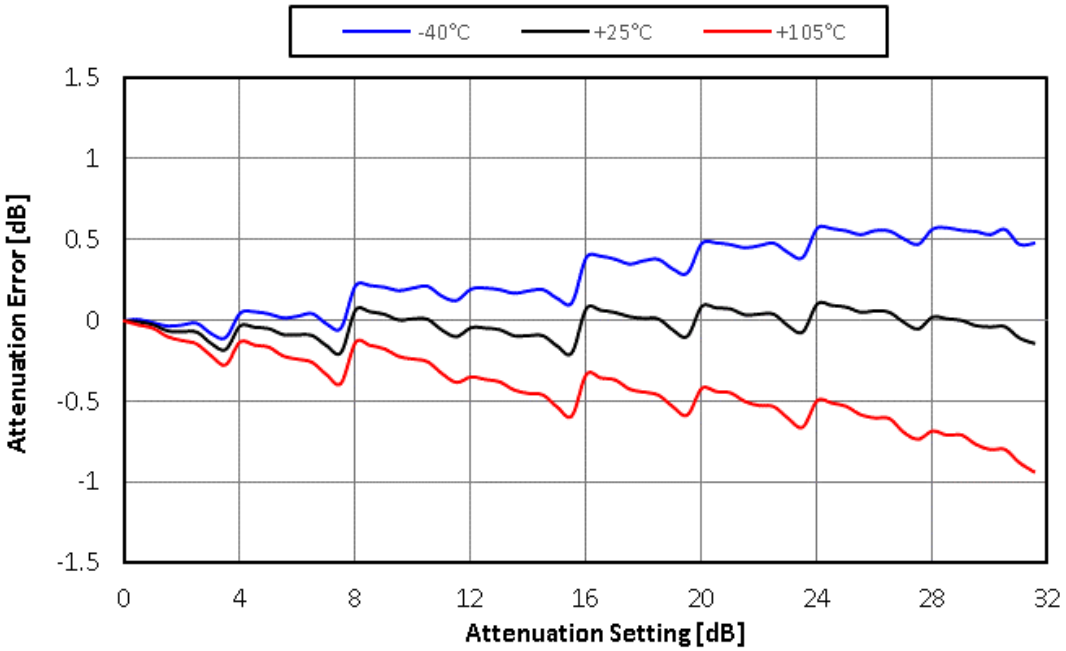
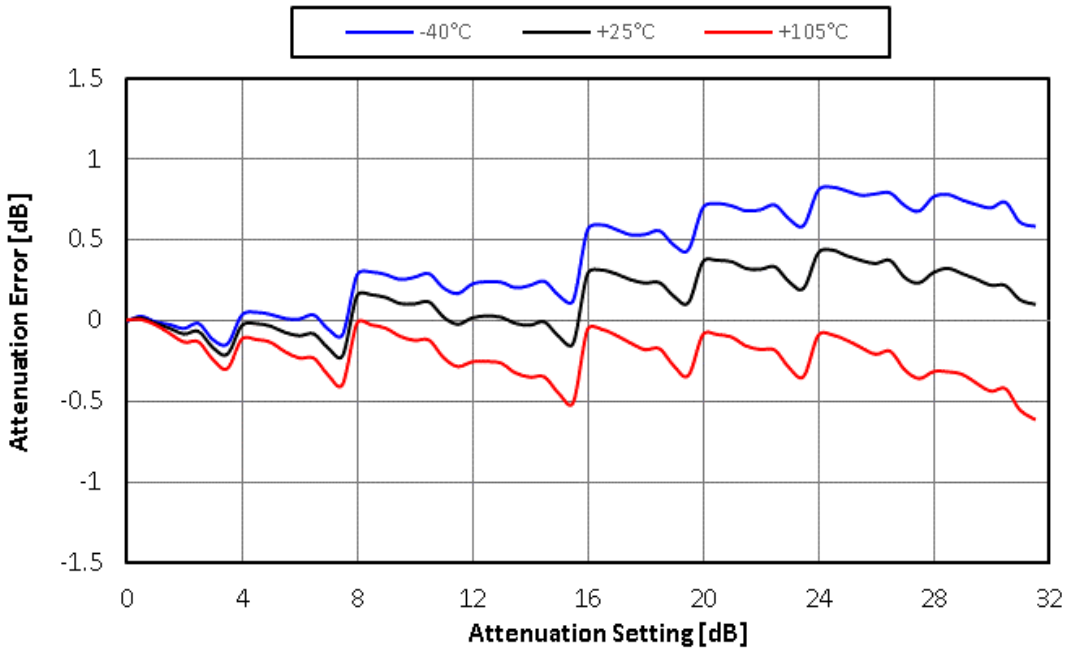


Figure 17. Attenuation Error @3500MHz vs Temperature



Typical RF Performance Plot - BDA4601 EVK - PCB

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit Rev.2 RF connector and board losses are de-embedded, unless otherwise noted

Figure 18. IIP3 @ 1950MHz vs Temperature

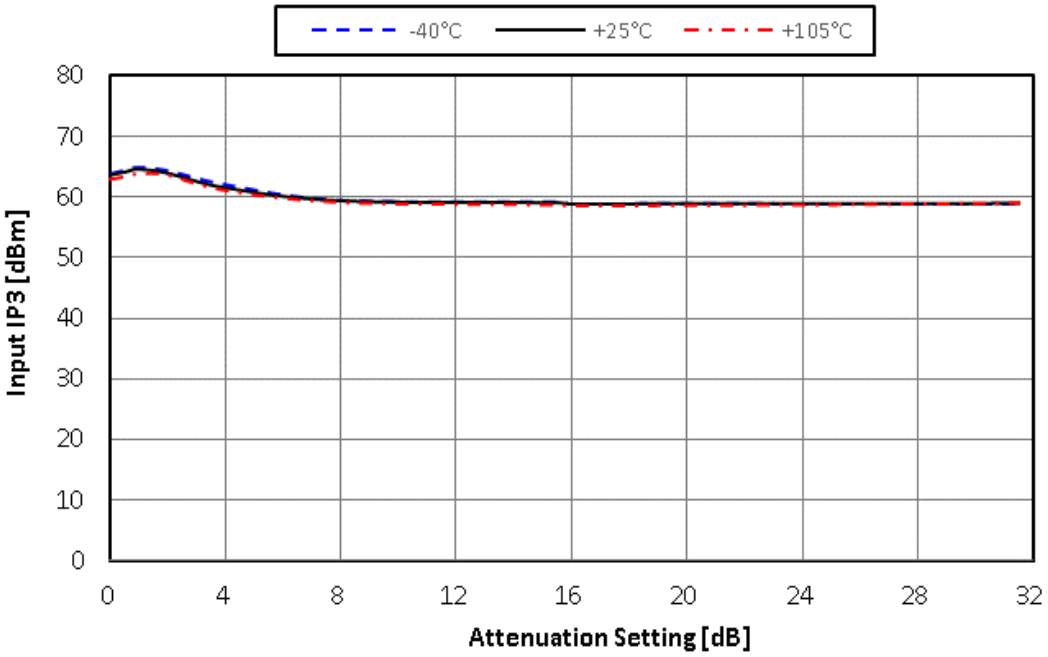
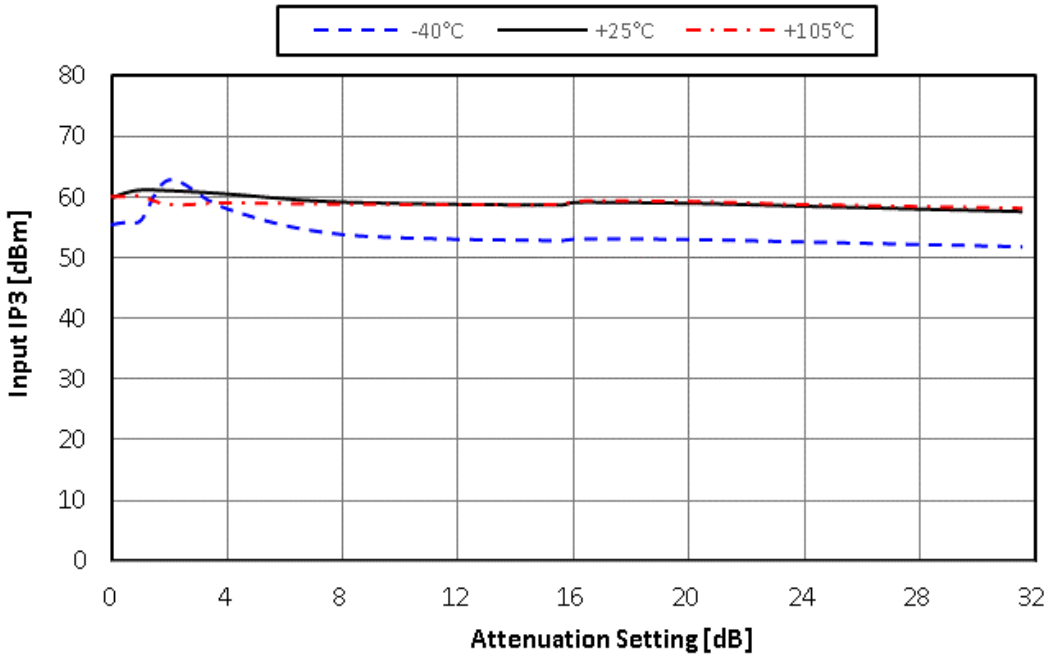


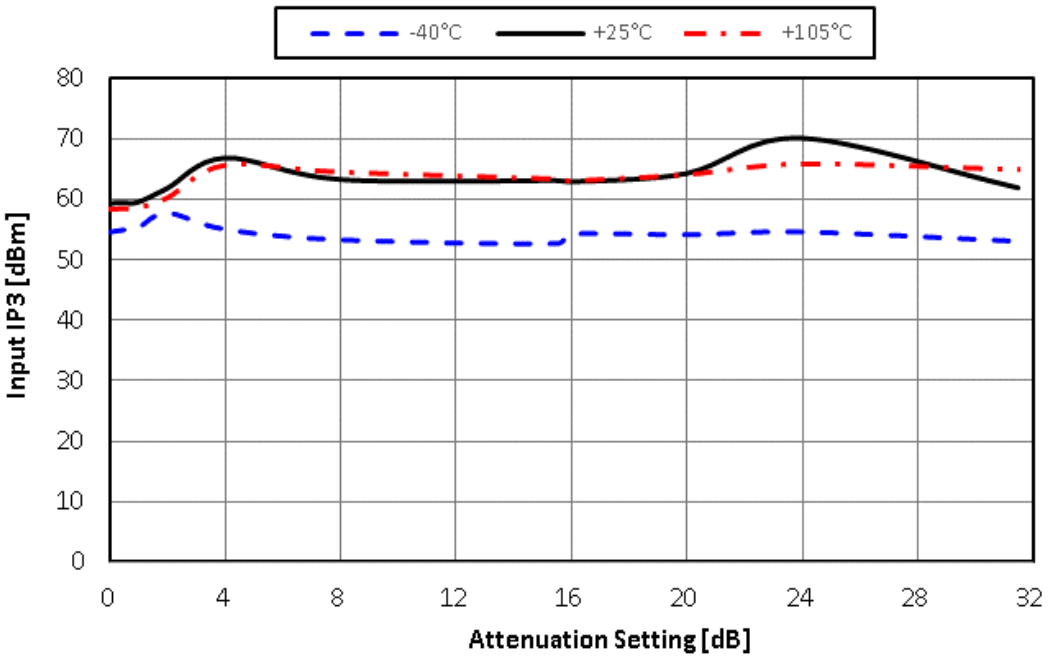
Figure 19. IIP3 @ 2650MHz vs Temperature



Typical RF Performance Plot - BDA4601 EVK - PCB

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit Rev.2 RF connector and board losses are de-embedded, unless otherwise noted

Figure 20. IIP3 @ 3500MHz vs Temperature



Typical RF Performance Plot - BDA4601 EVK - PCB

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit Rev.2 RF connector and board losses are de-embedded, unless otherwise noted

Figure 21. 0.1dB Compression @1950MHz vs Temperature

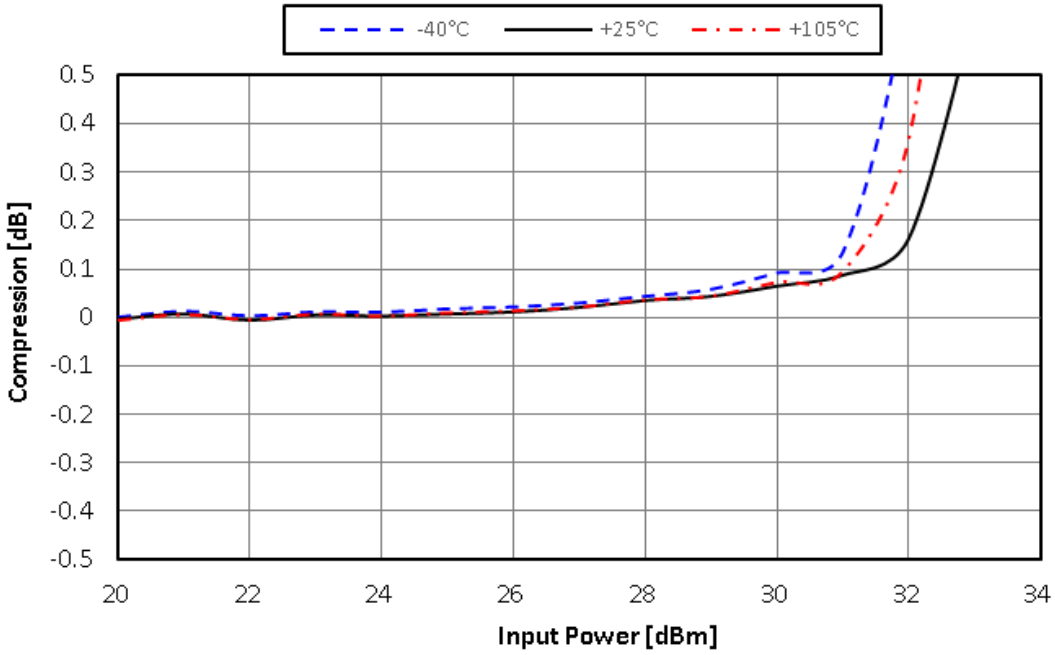
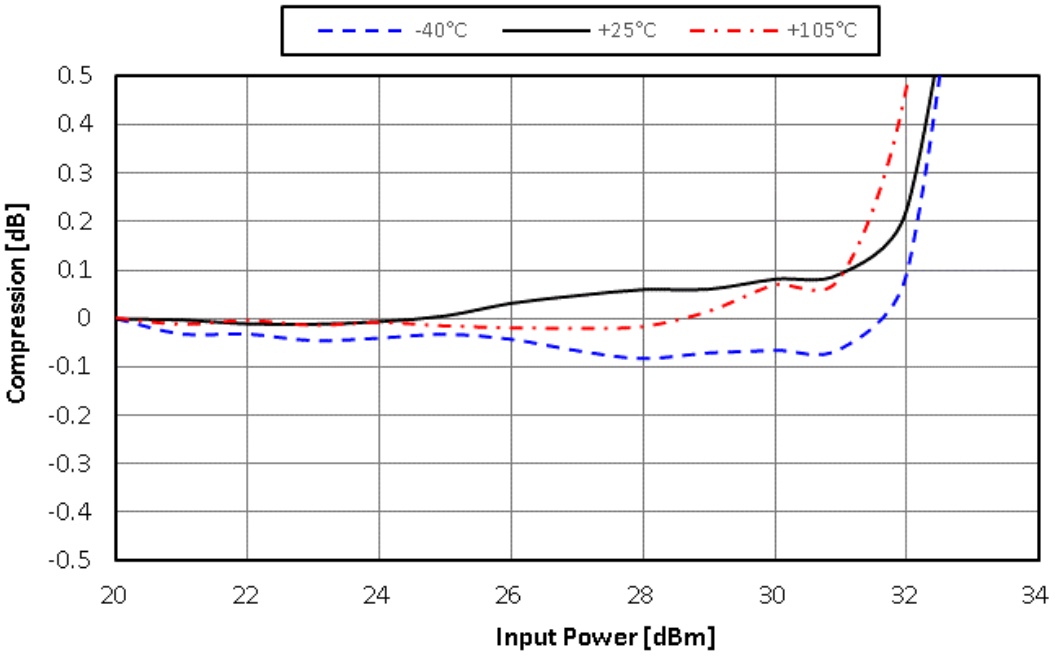


Figure 22. 0.1dB Compression @3500MHz vs Temperature



Typical RF Performance Plot - BDA4601 EVK - PCB

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit Rev.2 RF connector and board losses are de-embedded, unless otherwise noted

Figure 23. 0.5dB Step Attenuation vs Frequency

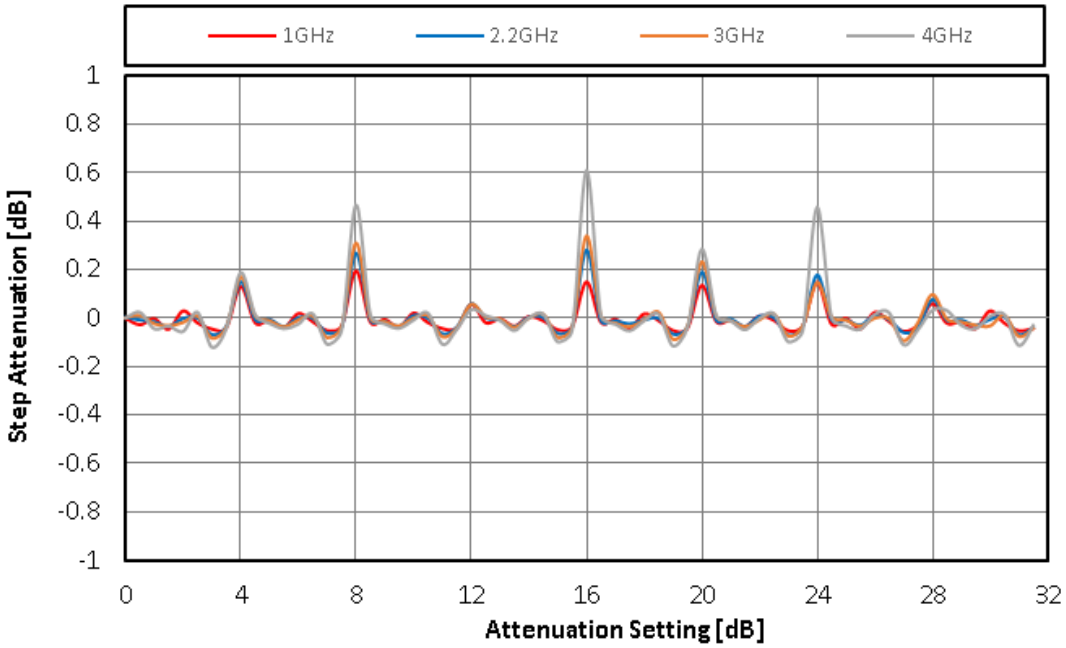
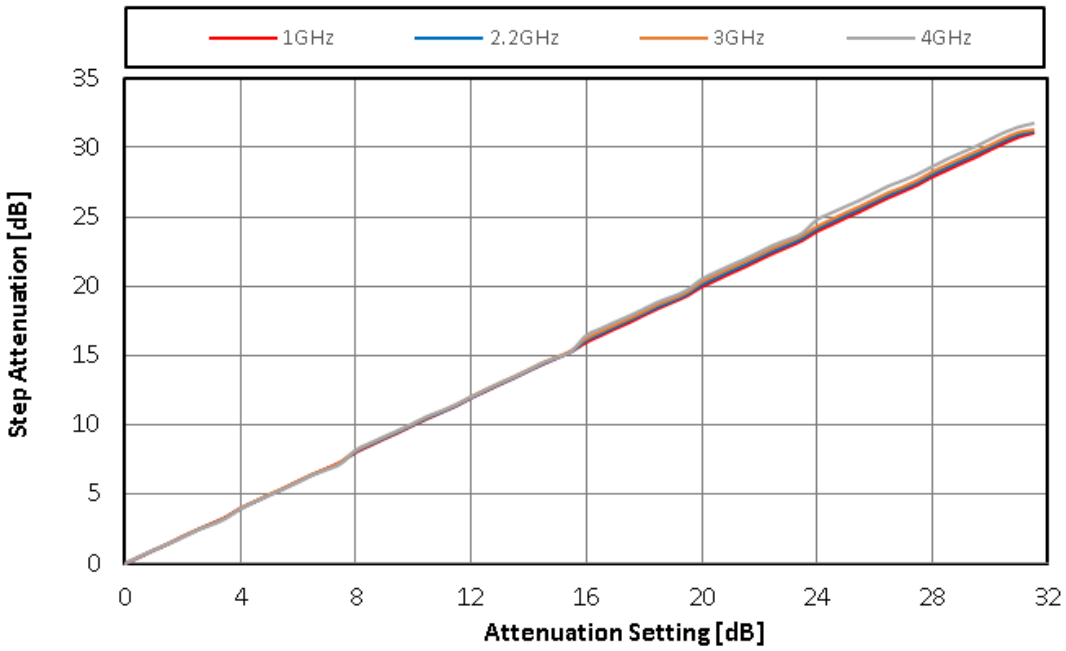


Figure 24. 0.5dB Step Attenuation vs Frequency



Typical RF Performance Plot - BDA4601 EVK - PCB

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit Rev.2 RF connector and board losses are de-embedded, unless otherwise noted

Figure 25. 0.5dB Major State Bit Error vs Attenuation Setting

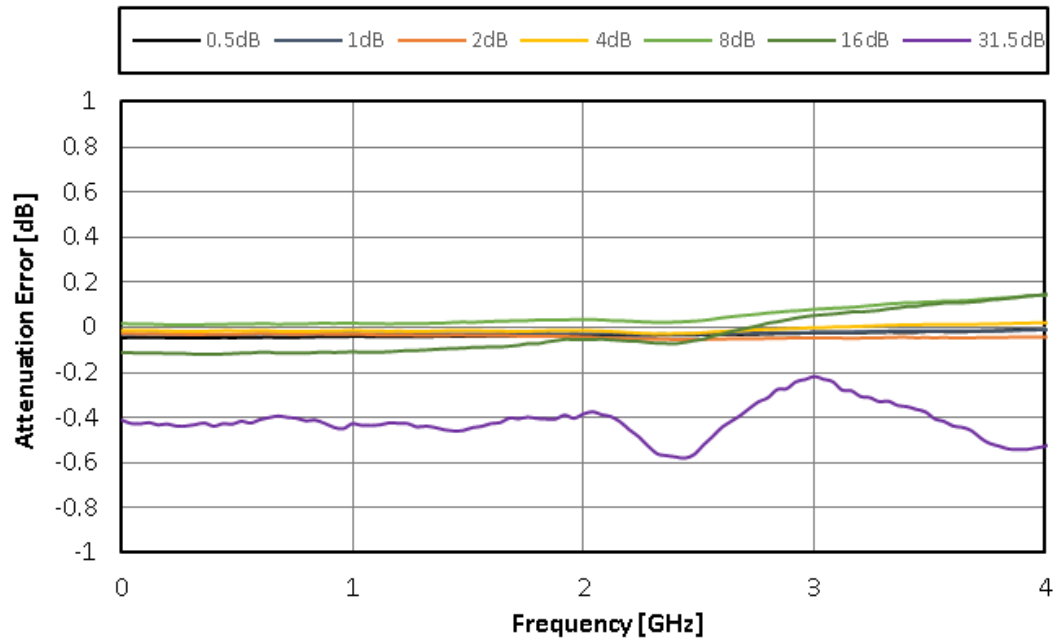
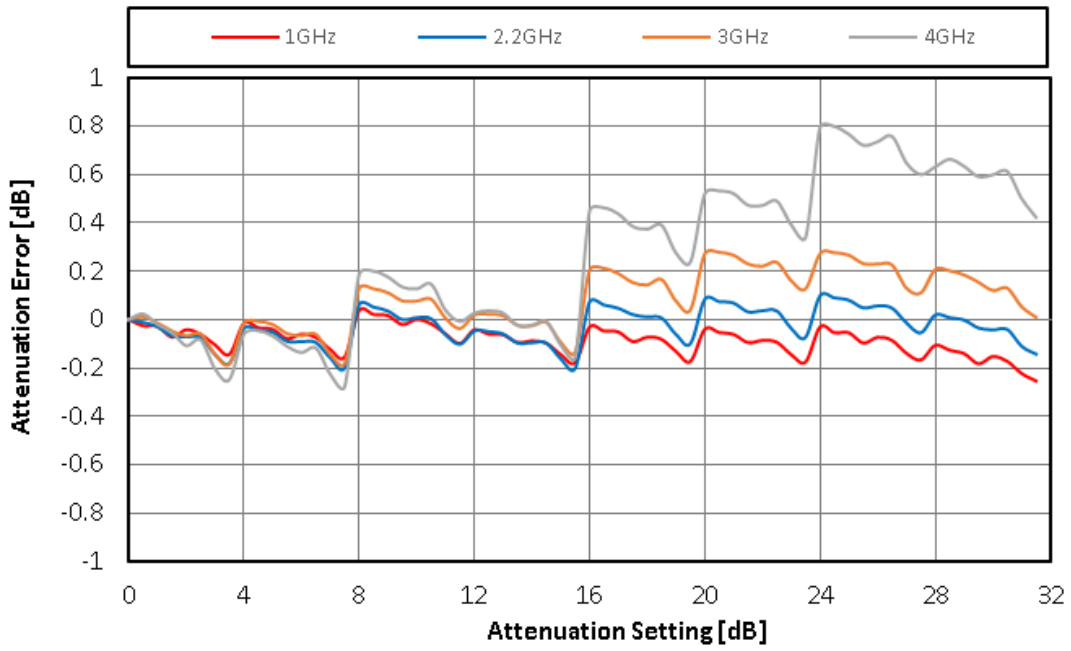


Figure 26. 0.5dB Major Attenuation Error vs Frequency



BDA4601 Evaluation board Kit Description

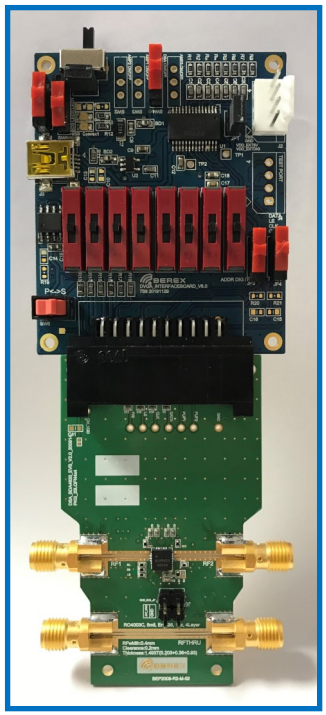


Figure 27. BDA4601 EVK Rev.2

Evaluation board Kit Introduction

BDA4601 Evaluation Kit is made up of a combination of an RF board and an interface board

The schematic of the BDA4601 evaluation RF board is shown in Figure 30. The BDA4601 evaluation RF board is constructed of a 4-layer material with a copper thickness of 0.7 mil on each layer. Every copper layer is separated with a dielectric material. The top dielectric material is 12 mil RO4003. The middle and bottom dielectric materials are FR-4, used for mechanical strength and overall board thickness of approximately 1.55mm.
BDA4601 Evaluation INTERFACE board is assembled with a SP3T switches(D0~D5, LE), SP2T mechanical switch (P/S), and several header & switch.

Evaluation Board Programming Using USB Interface

In order to evaluate the BDA4601 performance, the Application Software has to be installed on your computer. And The DSA application software GUI supports Latched Parallel and Serial modes. software can be downloaded from BeRex's website

Serial Control Mode

- Connect directly the Evaluation INTEFRACE board USB port(J3) to PC
- Set the direction of P<->S Switch to S direction
- Set the D0~D5,LE switch to the central position.
- Operate the 0~31.5dB attenuation state in GUI and then control the DSA

Latched Parallel Control Mode

- Connect directly the Evaluation INTEFRACE board USB port(J3) to PC
- Set the direction of P<->S Switch to P direction
- Set the D0~D5,LE switch to the middle position.
- Operate the 0~31.5dB attenuation state in GUI and then control the DSA

Direct Parallel Control Mode

- Set the direction of P<->S Switch to P direction
- Set LE switch to the LOW Position
- For the setting to attenuation state, D0~D5 switches can be combined in manually program, refer to Table 10.

Please refer to User Manual Rev.1 or Rev.2 for more detailed operation method of BDA4601 EVK.

BDA4601 Evaluation board Kit Rev.2 Description

Figure 28. Evaluation Board Kit Schematic Diagram

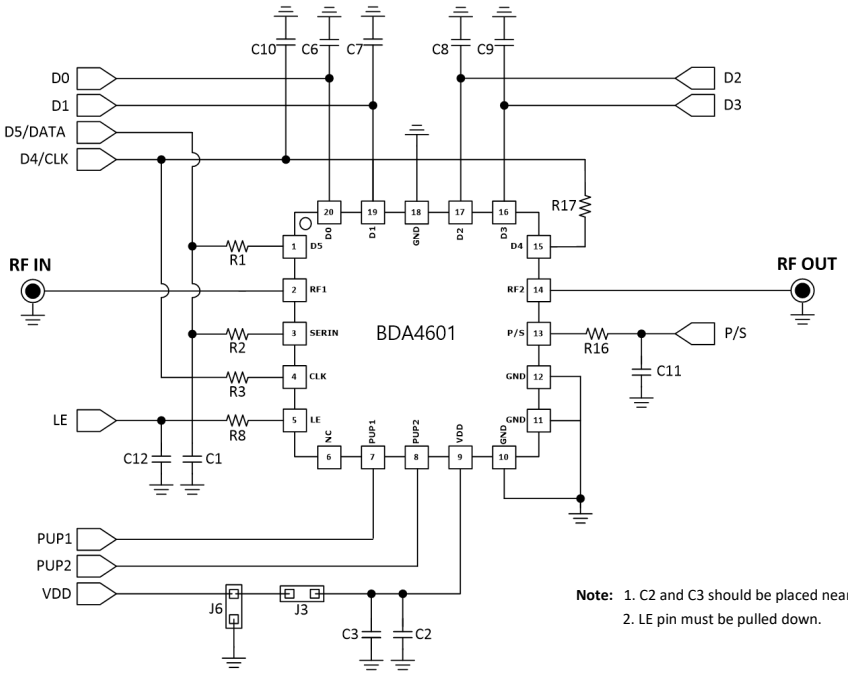


Figure 29. Evaluation Board PCB Layout Information

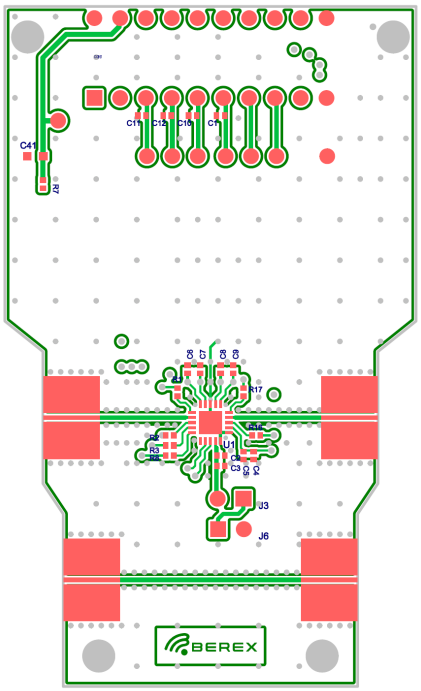
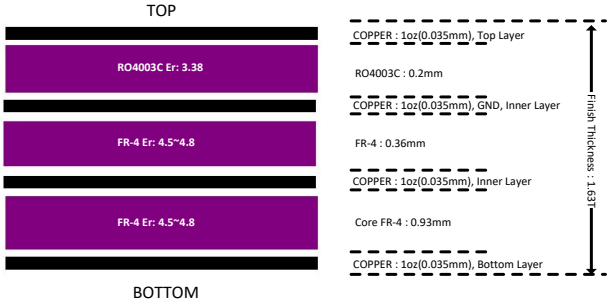


Table 14. Bill of Material - Evaluation Board

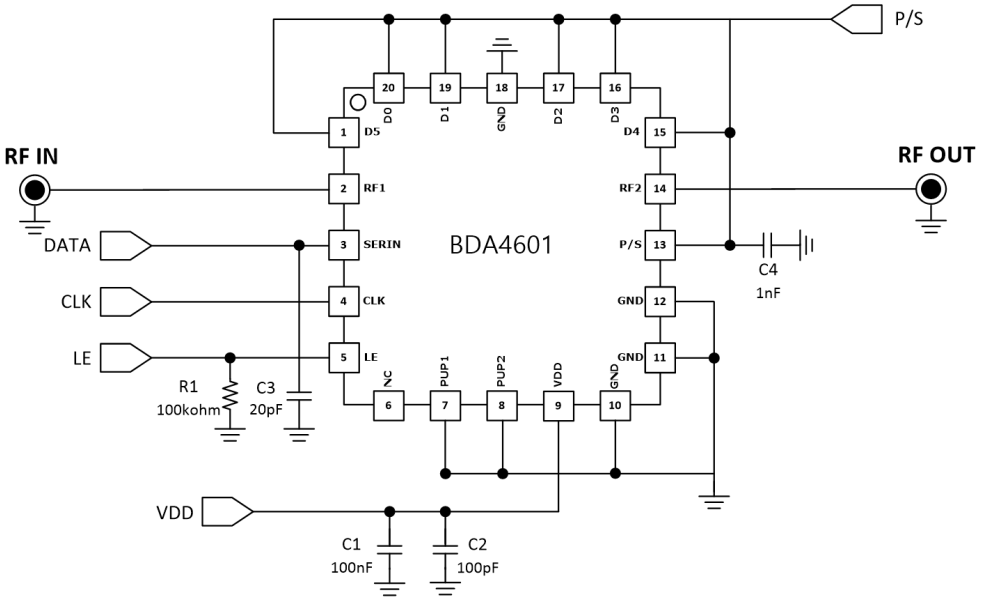
No.	Ref Des	Part Qty	Value	Description	Remark
1	C1,C2,C6-C12	9	100pF	CAP, 0402, CHIP Ceramic, ±0.25%	
2	C3	1	100nF	CAP, 0402, CHIP Ceramic, ±0.25%	
3	R1,R16,C4	2	0 ohm	RES, 0402, CHIP, ±5%	
4	C5,C41,R7	1	NC		
4	R2,R3,R8,R17	2	1k ohm	RES, 0402, CHIP, ±5%	
5	SMA1, SMA2	2	CON	SMA END LAUNCH	
6	U1	1	Chip	DSA, BDA4601 QFN4x4 24L	

Figure 30. Evaluation Board PCB Layer Information



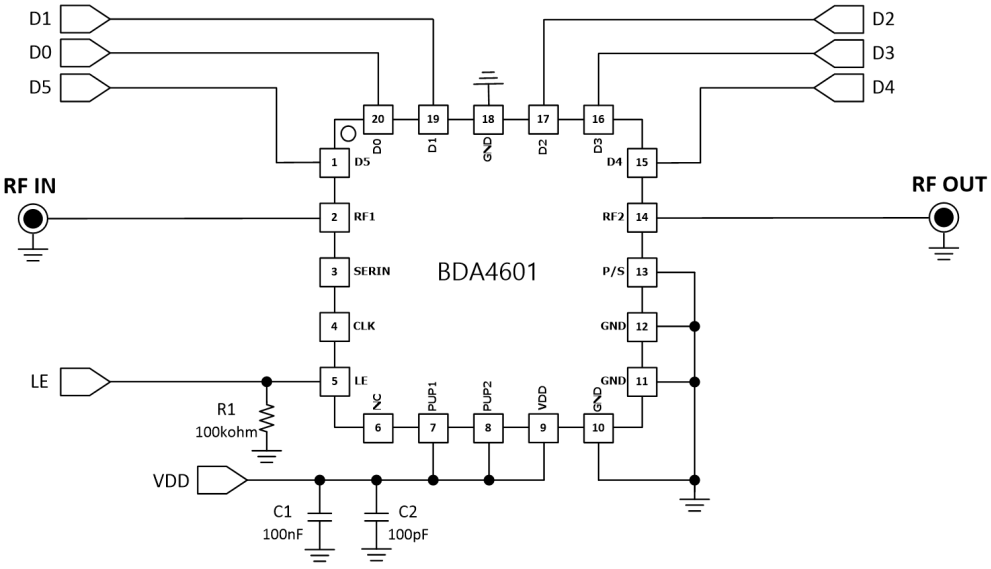
BDA4601 Evaluation board Kit Description

Figure 31. Serial mode Application Schematic (Max Attenuation Power Up State)



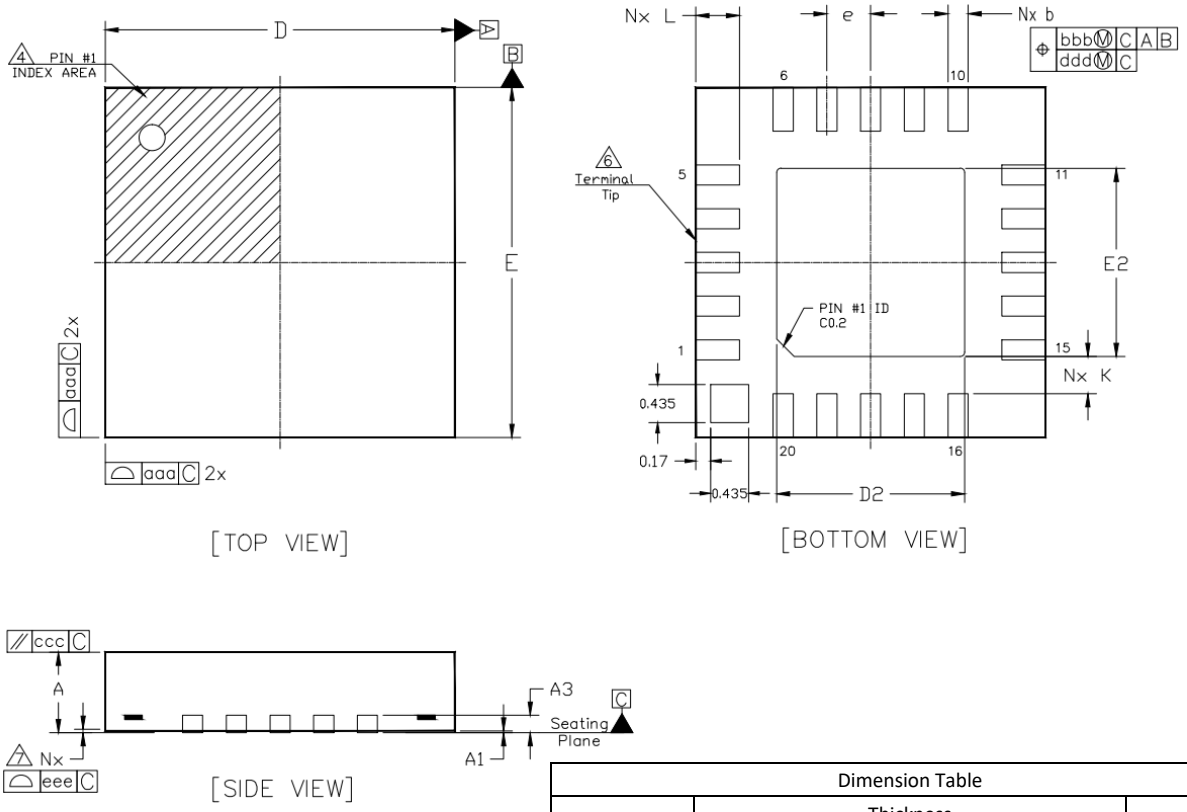
Note: 1. C1 ~ C4 should be placed near the device.
2. LE pin must be set to Logic Low for Maximum Attenuation to operate during power-up. Recommended to add pull-down resistor(R1) at the LE pin.

Figure 32. Latched Parallel mode Application Schematic (Max Attenuation Power Up State)



Note: 1. C1 and C2 should be placed near the device.
2. LE pin must be set to Logic Low for Maximum Attenuation to operate during power-up. Recommended to add pull-down resistor(R1) at the LE pin.

Figure 33. Packing Outline Dimension



NOTE :

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.

2. All dimensions are in millimeters.

3. N is the total number of terminals.

4. The location of the marked terminal #1 identifier is within the hatched area.

5. ND and NE refer to the number of terminals on each D and E side respectively.

6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.

7. Coplanarity applies to the terminals and all other bottom surface metallization

Dimension Table				
Symbol	Thickness			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.203 Ref	---	
b	0.18	0.23	0.28	6
D		4.00 BSC		
E		4.00 BSC		
e		0.50 BSC		
D2	2.10	2.15	2.20	
E2	2.10	2.15	2.20	
K	0.20	---	---	
L	0.45	0.55	0.65	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		20		3
ND		5		5
NE		5		5

Figure 34. Recommend Land Pattern

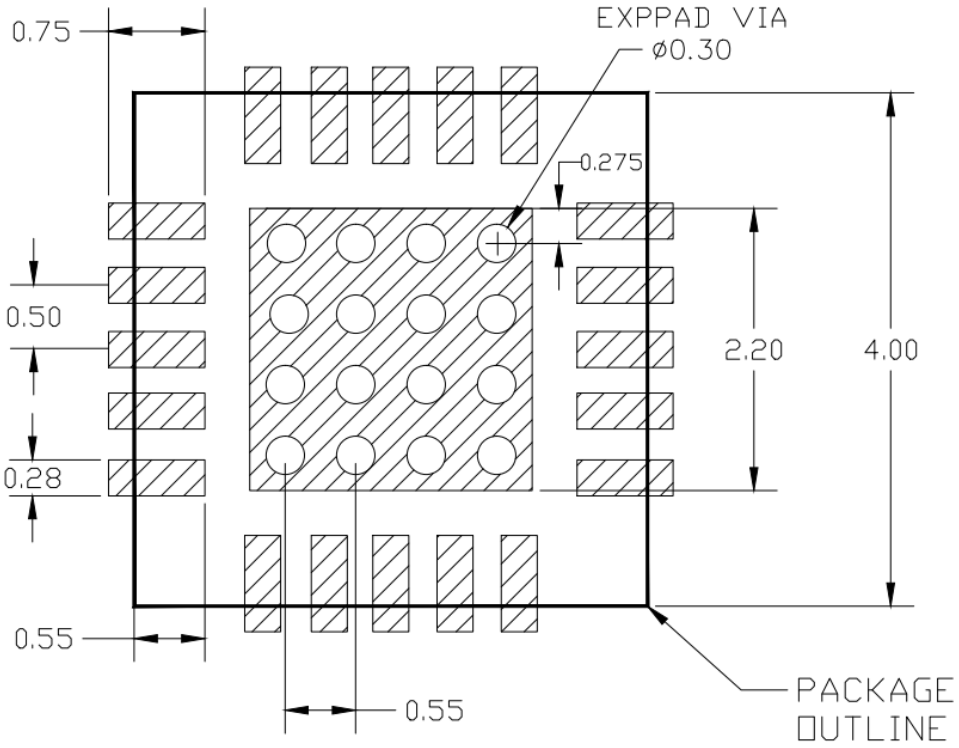
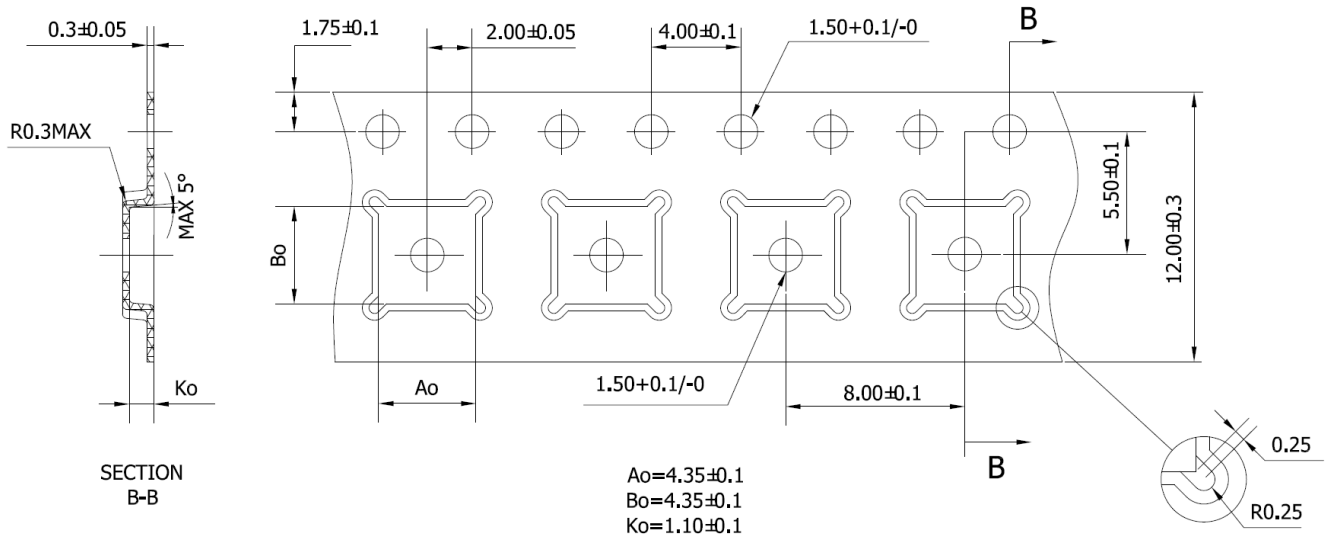


Figure 35. Package Marking

Marking information:	
BDA4601	Device Name
YY	Year
WW	Work Week
XX	LOT Number

Figure 36. Tape & Reel



NOTES:
1 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2 CAMBER IN COMPLANCE WITH EIA 481
3 POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET,NOT POCKET HOLE

Packaging information:	
Tape Width	12mm
Reel Size	7inch
Device Cavity Pitch	8mm
Devices Per Reel	1k

Lead plating finish

100% Tin Matte finish

MSL / ESD Rating

ESD Rating:	Class 2
Value:	±2000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JS-001-2017
MSL Rating:	**Level 1 at +260°C convection reflow**
Standard:	JEDEC Standard J-STD-020

Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

2	**N**	**9**	**6**	**F**