BDA4620

6-bit Digital Step Attenuator

1MHz – 8000MHz

Device Features

- 6-bit Serial & Parallel Interface
- 31.5 dB Control Range 0.5 dB step
- Glitch-safe attenuation state transitions
- 2.7 V to 5.5 V supply
- 1.8 V or 3.3 V control logic
- Excellent Attenuation Accuracy
  - ±(0.15 + 1.5% of attenuation state) @ 1.9GHz
  - ±(0.25 + 3.5% of attenuation state) @ 3.5GHz
  - ±(0.35 + 7.0% of attenuation state) @ 7.2GHz
- Low Insertion Loss
  - 0.9 dB @ 1.9GHz
  - 1.2 dB @ 3.5GHz
  - 2.4 dB @ 7.2GHz (Optimized Application)
- Ultra linearity IIP3 > +63 dBm @ 3.5GHz, ATT=0dB
- Input 0.1dB Compression (P0.1dB) 30dBm @ 3.5GHz, ATT=0dB
- Programming modes
  - Direct parallel
  - Latched parallel
  - Serial
- Stable Integral Non-Linearity over temperature
- Low Current Consumption 200 µA typical
- -40 °C to +105 °C operating temperature
- ESD rating : Class1C (1kV HBM)
- Lead-free/RoHS2-compliant 20-lead 4mm x 4mm x 0.9mm QFN SMT package

20-lead 4mm x 4 mm x 0.9mm QFN

Figure 1. Package Type

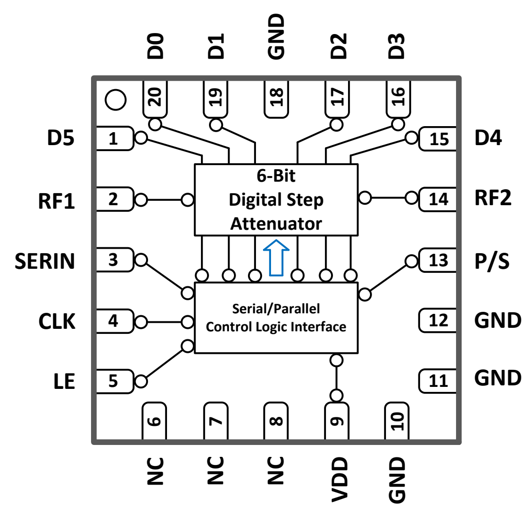


Figure 2. Functional Block Diagram

Product Description

The BDA4620 is a broadband, Highly accurate 50Ω digital step attenuator model which provides adjustable attenuation from 0 to 31.5 dB in 0.5 dB steps. The control is a 6-bit serial interface and latched parallel interface.

BDA4620 supports a broad operating frequency range from 1MHz to 8.0 GHz. BDA4620 is offering the High linearity, low power consumption, low insertion loss and high attenuation accuracy at all frequency band.
The device features a safe state transitions with no negative/positive Glitch technology optimized for excellent step accuracy.

Basically the RF input and output are internally matched to 50Ω and do not require any external matching components. Besides there is no need for DC blocking Capacitor If DC is not presented at the RF Port .
In some cases to optimized Return loss for above 4 - 8GHz, Shunt capacitor can be added near RF1 and RF2 respectively.
The design is bi-directional; therefore, the RF input and output are interchangeable.

This DSA does not require blocking capacitors. If DC is presented at the RF port, add a blocking capacitor.
It is packaged in a RoHS2-compliant with QFN surface mount package.

Application

- 6G/5G/4G/3G Cellular Base station/Repeater Infrastructure
- Digital Pre-Distortion
- Distributed Antenna Systems, DAS
- Remote Radio Heads
- NFC Infrastructure
- Test Equipment and sensors
- Military Wireless system
- Cable Infrastructure
- General purpose Wireless

Rev. 2.1

Table 1. Electrical Specifications

Specifications are performance on the BeRex EVKit at VDD=3.3V, 25°C, 50Ω system. Performance were measured based on Typical application circuits Table 12. (See the Page 9)

Parameter		Condition	Frequency	Min	Typ	Max	Unit
Operating Frequency Range				1		6000	MHz
Attenuation Range		0.5dB step			0 - 31.5		dB
Insertion Loss[1]		ATT = 0dB	1MHz - 1GHz		0.7		dB
			1 - 2GHz		0.9		dB
			2 - 3GHz		1.1		dB
			3 - 4GHz		1.3		dB
			4 - 6GHz		2.7		dB
Attenuation Error		0-31.5dB / 0.5dB Step	1MHz - 1GHz			±(0.10 + 1.0% of attenuation state)	dB
			1 - 2GHz			±(0.15 + 1.5% of attenuation state)	dB
			2 - 3GHz			±(0.15 + 2.5% of attenuation state)	dB
			3 - 4GHz			±(0.25 +3.5% of attenuation state)	dB
			4 - 6GHz			±(0.25 +5.0% of attenuation state)	dB
Input Return Loss		ATT = 0dB	1 - 4GHz		20		dB
			4 - 6GHz		10		
Output Return Loss		ATT = 0dB	1 - 4GHz		21		dB
			4 - 6GHz		11		
Relative Phase Error		All states	1GHz		7		degree
			2GHz		15		
			3GHz		24		
			4GHz		33		
			5GHz		41		
			6GHz		50		
Input Linearity	Input 0.1dB Compression Point	ATT = 0dB	3.5GHz		30		dBm
	Input IP3	Pin = +18dBm/tone, △f = 10kHz ATT = 0.0dB RF Input = RF1 Port	2.5GHz		52		dBm
			3.5GHz		63		
			4.5GHz		56		
		Pin = +18dBm/tone, △f = 10kHz ATT = 31.5dB RF Input = RF1 Port	2.5GHz		58		dBm
			3.5GHz		54		
			4.5GHz		53		
		Pin = +18dBm/tone, △f = 10kHz ATT = 0.0dB RF Input = RF2 Port	2.5GHz		57		dBm
			3.5GHz		60		
			4.5GHz		55		
		Pin= +18dBm/tone, △f = 10kHz ATT = 31.5dB RF Input = RF2 Port	2.5GHz		46		dBm
			3.5GHz		56		
			4.5GHz		55		
RF Rising / Falling Time		10%/90% RF	2GHz		110		ns
Switching Time		50% LE Control to 90% or 10% RF	2GHz		210		ns
Settling Time		50% LE to Max or Min Attenuation to settle within 0.05 dB of final value	2GHz		400		ns
Attenuation Transient(envelope)[2]		Positive Glitch, Any ATT step			0.3		dB
Maximum Spurious Level		Measured at RF1 and RF2 port	1 - 5MHz		-116		dBm/10Hz
			>5MHz[3]		< -145		

1. The Evaluation board Kit insertion loss (PCB & RF Connector) is de-embedded.
2. Attenuation Transient is glitch level due to attenuation transitions.
3. No spurious signals were detected above 5MHz.

Table 2. Electrical Specifications[1] (Optimized Return Loss Application)

Specifications are performance on the BeRex EVKit at VDD=3.3V, 25°C, 50 Ω system. Performance were measured based on Optimized Return Loss Application Circuits Table 13. (See the Page 14)

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating Frequency Range			1		8000	MHz
Attenuation range	0.5dB step			0 - 31.5		dB
Insertion Loss[2]	ATT = 0dB	1MHz - 1GHz		0.6		dB
		1 - 2GHz		0.9		dB
		2 - 3GHz		1.1		dB
		3 - 4GHz		1.1		dB
		4 - 6GHz		1.7		dB
		6 - 8GHz		2.8		dB
Attenuation Error	0-31.5dB / 0.5dB Step	1MHz - 1GHz			±(0.10 + 1.0% of attenuation state)	dB
		1 - 2GHz			±(0.15 + 1.5% of attenuation state)	dB
		2 - 3GHz			±(0.15 + 2.5% of attenuation state)	dB
		3 - 4GHz			±(0.25 +3.5% of attenuation state)	dB
		4 - 6GHz			±(0.25 +5.0% of attenuation state)	dB
		6 - 8GHz			±(0.35 +7.0% of attenuation state)	dB
Input Return Loss	ATT = 0dB	1 - 4GHz		14		dB
		4 - 6GHz		19		
		6 - 8GHz		20		
Output Return Loss	ATT = 0dB	1 - 4GHz		16		dB
		4 - 6GHz		20		
		6 - 8GHz		23		
Relative Phase Error	All states	1GHz		7		degree
		2GHz		15		
		3GHz		24		
		4GHz		33		
		5GHz		41		
		6GHz		50		
		7GHz		57		
		8GHz		79		

1. In order to improve Return loss above 4GHz, shunt capacitor 0.1pF was added to each RF1 & RF2. (See Optimized Return loss application circuits Table 13 on page 14)
2. The Evaluation board Kit insertion loss (PCB & RF Connector) is de-embedded.

Table 3. Recommended Operating Condition

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Supply Voltages		V_{DD}		2.7		5.5	V
Supply Current		I_{DD}			200	310	µA
Digital Control Input	**High**	V_{CTLH}	V_{DD}=3.3V or 5V	1.17		3.6	V
	Low	V_{CTLL}	V_{DD}=3.3V or 5V	-0.3		0.6	V
Operating Temperature Range		T_{case}	Exposed Paddle	-40		105	˚C
RF Max Input Power		P_{IN_CW}	RF1 or RF2, CW (> 50MHz)			24	dBm
Impedance		Z_{Load}	Single ended		50		Ω

Specifications are not guaranteed over all recommended operating conditions.

Table 4. Absolute Maximum Ratings

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{DD}	-0.3		5.5	V
Digital Input Voltage		V_{CTL}	-0.3		3.6	V
Maximum Input Power		P_{IN_CWMAX}			31	dBm
Temperature	**Storage**	T_{ST}	-65		150	℃
	Reflow	T_R			260	℃
ESD Sensitivity	**HBM**[1]	ESD_{HBM}			±1000 (Class 1C)	V
	CDM[2]	ESD_{CDM}			±1000 (Class C3)	V

Operation of this device above any of these parameters may result in permanent damage.
1. HBM : Human Body Model (JEDEC **Standard JS-001-2017**)
2. CDM : Charged Device Model (JEDEC **Standard JS-002-2018**)

Table 5. Package Thermal Characteristics

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	37.4	°C/W

Figure 3. Pin Configuration (Top View)

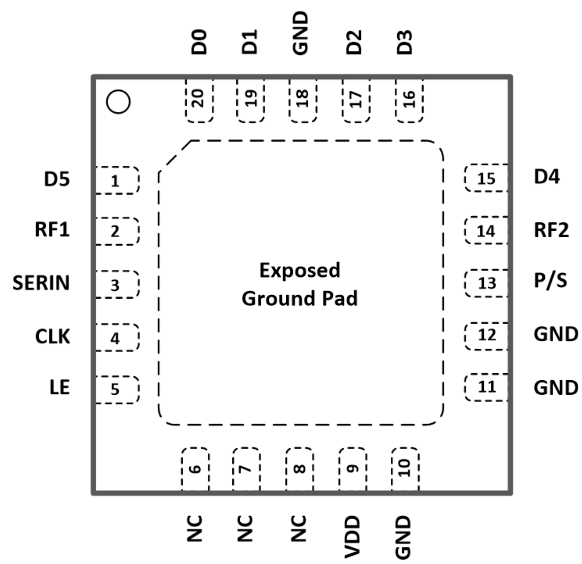


Table 6. Pin Descriptions

Pin	Pin name	Description
1	D5[2]	Attenuation control bit, 16dB
2	RF1[1]	RF1 port (Attenuator RF Input) This pin can also be used as an output because the design is bi-directional. RF1 is dc-coupled and matched to 50 Ω
3	SERIN	Serial interface data input
4	CLK	Serial interface clock input
5	LE	Latch Enable input
6, 7, 8	NC	Not Connected
9	VDD	Power Supply (nominal 3.3V)
10, 11, 12, 18	GND	Ground, These pins must be connected to ground
13	P/S	Parallel/Serial Mode Select. For parallel mode operation, set this pin to LOW. For serial mode operation, set this pin to HIGH.
14	RF2[1]	RF2 port (Attenuator RF Output.) This pin can also be used as an input because the design is bi-directional. RF2 is dc-coupled and matched to 50 Ω.
15	D4[2]	Attenuation control bit, 8dB
16	D3[2]	Attenuation control bit, 4dB
17	D2[2]	Attenuation control bit, 2dB
19	D1[2]	Attenuation control bit, 1dB
20	D0[2]	Attenuation control bit, 0.5dB
Pad	GND	Exposed pad: The exposed pad must be connected to ground for proper operation

1. RF pins 2 and 14 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met.
2. Ground D0 - D5 if not in use or serial mode.

Programming Options

BDA4620 can be programmed using either the parallel or serial interface, which is selectable via P/S pin(Pin13).
Serial mode is selected by pulling it to a voltage logic HIGH and parallel mode is selected by setting P/S to logic LOW

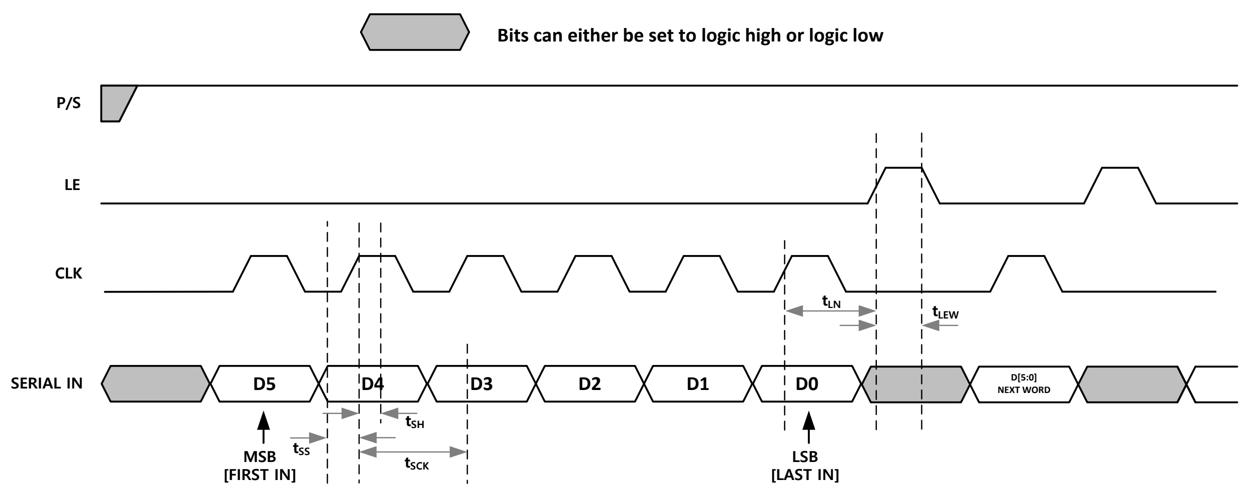
Serial Control Mode

The serial interface is a 6-bit shift register to shift in the data MSB (D5) first. When serial programming is used, It is recommended all the parallel control input pins (1, 15, 16, 17, 19, 20) are grounded.
It is controlled by three CMOS-compatible signals: SERIN, Clock, and Latch Enable (LE).

Table 7. Truth Table for Serial Control Word

Digital Control Input						Attenuation state (dB)
D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	
LOW	LOW	LOW	LOW	LOW	LOW	0 (RL)
LOW	LOW	LOW	LOW	LOW	**HIGH**	0.5
LOW	LOW	LOW	LOW	**HIGH**	LOW	1
LOW	LOW	LOW	**HIGH**	LOW	LOW	2
LOW	LOW	**HIGH**	LOW	LOW	LOW	4
LOW	**HIGH**	LOW	LOW	LOW	LOW	8
HIGH	LOW	LOW	LOW	LOW	LOW	16
HIGH	**HIGH**	**HIGH**	**HIGH**	**HIGH**	**HIGH**	31.5

Figure 4. Serial Mode Timing Diagram



The BDA4620 has a 3-wire serial peripheral interface (SPI): serial data input (SERIN), clock (CLK), and latch enable (LE). The serial control interface is activated when P/S is set to HIGH.
In serial mode, the 6-bit Data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggled HIGH to latch the new attenuation state into the device. LE must be set to LOW to clock new 6-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept HIGH (see Figure 4 and Table 7).

Table 8. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{CLK}	Serial data clock frequency			10	MHz
t_{SCK}	Minimum serial period	70			ns
t_{SS}	Serial Data setup time	10			ns
t_{SH}	Serial Data hold time	10			ns
t_{LN}	LE setup time	10			ns
t_{LEW}	Minimum LE pulse width	30			ns

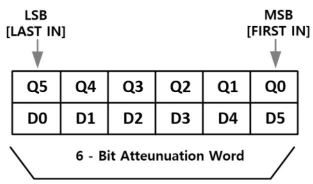
Table 9. Mode Selection

P/S	Control Mode
LOW	**Parallel**
HIGH	**Serial**

Serial Register Map

The BDA4620 can be programmed via the serial control on the rising edge of Latch Enable (LE) which loads the last 6-bits data word in the SHIFT Register. Data is clocked in MSB(D5) first.

Figure 5. Serial Register Map



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by two, then convert to binary.
For example, to program the 15.5dB state :

2 x 15.5 = 31
D0 — D5 : 111110

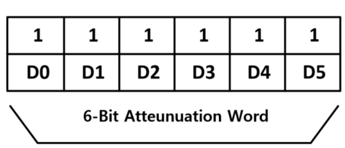
Serial Input : 111110

1	1	1	1	1	0
D0	D1	D2	D3	D4	D5

Power-UP states Settings

The BDA4620 will always initialize to the maximum attenuation setting (31.5 dB) on power-up for both the Serial and Latched Parallel modes of operation and will remain in this setting until the user latches in the next programming word.
In Direct Parallel mode, the DSA can be preset to any state within the 31.5 dB range by pre-setting the Parallel control pins prior to power-up. In this mode, there is a 400 µs delay between the time the DSA is powered-up to the time the desired state is set.

Figure 6. Default Attenuation word for Power-up state



Programming Options

Parallel Control Mode

The parallel control interface has seven digital control input lines (D5 to D0) to set the attenuation value. D5 is the most significant bit (MSB) that selects the 16 dB attenuator stage, and D0 is the least significant bit (LSB) that selects the 0.5 dB attenuator stage.

Direct Parallel Mode

For direct parallel mode, The LE pin must be kept HIGH. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 1, 15, 16, 17, 19, 20]. Use direct parallel mode for the fastest settling time.

Latched Parallel Mode

The LE pin must be kept LOW when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled HIGH to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled LOW to latch the change into the device until the next desired attenuation change (see Figure 7 and Table 10).

- Set P/S is logic LOW.
- Set LE to logic LOW.
- Adjust pins [1, 15, 16, 17, 19, 20] to the desired attenuation setting. (Note the device will not react to these pins while LE is a logic LOW).
- Pull LE to a logic HIGH. The device will then transition to the attenuation settings reflected by pins D5 - D0.
- If LE is pulled to a logic LOW then the attenuator will not change state.

Latched Parallel Mode implies a default state for when the device is first powered up with P/S pin set for logic LOW and LE logic LOW. In this case the default setting is **Maximum attenuation** .

Switching Feature Description

Glitch-Safe Attenuation State Transient

The BDA4620 is the latest product applied *Glitch-Safe* technology with less than 1dB ringing (pos/neg) across the attenuation range when changing attenuation states. This technology protects Amplifiers or ADC during transitions between attenuation states.
(see Figure 32,33).

Table 10. Truth Table for the Parallel Control Word

D5	D4	D3	D2	D1	D0	P/S	LE	Attenuation State(dB)
LOW	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	0 (RL)
LOW	LOW	LOW	LOW	LOW	HIGH	LOW	HIGH	0.5
LOW	LOW	LOW	LOW	HIGH	LOW	LOW	HIGH	1.0
LOW	LOW	LOW	HIGH	LOW	LOW	LOW	HIGH	2.0
LOW	LOW	HIGH	LOW	LOW	LOW	LOW	HIGH	4.0
LOW	HIGH	LOW	LOW	LOW	LOW	LOW	HIGH	8.0
HIGH	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	16.0
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	31.5

Figure 7. Latched Parallel Mode Timing Diagram

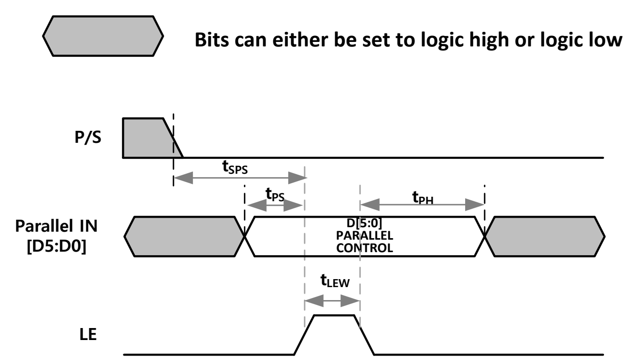


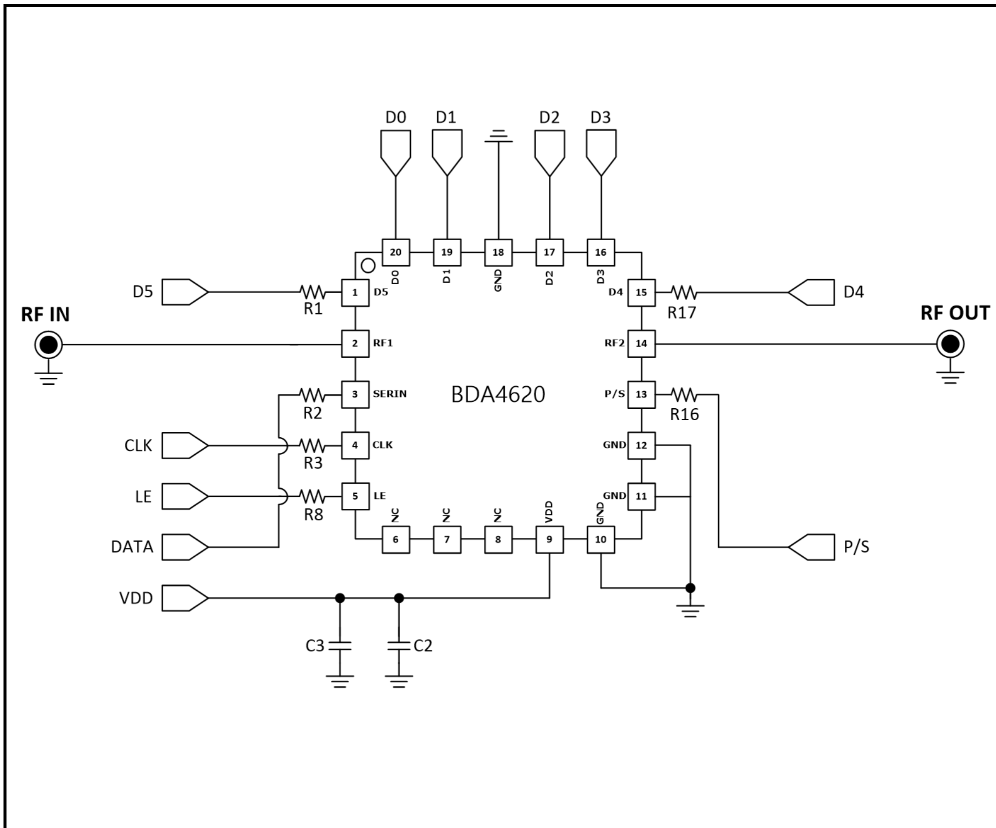
Table 11. Parallel Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_{SPS}	Serial to Parallel Mode Setup Time	100			ns
t_{LEW}	Minimum LE pulse width	10			ns
t_{PH}	Data hold time from LE	10			ns
t_{PS}	Data setup time to LE	10			ns

Typical RF Performance Plot - BDA4620 EVK - PCB (Typical Application Circuits)

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Table 12. Typical Application Circuits



BOM	
C2	100pF
C3	100nF
R1-R3,R8,R16,R17	1kohm

1. See the page 18 the Evaluation Board Circuits for the detailed application circuit information.

Figure 8. Insertion Loss vs Temp.

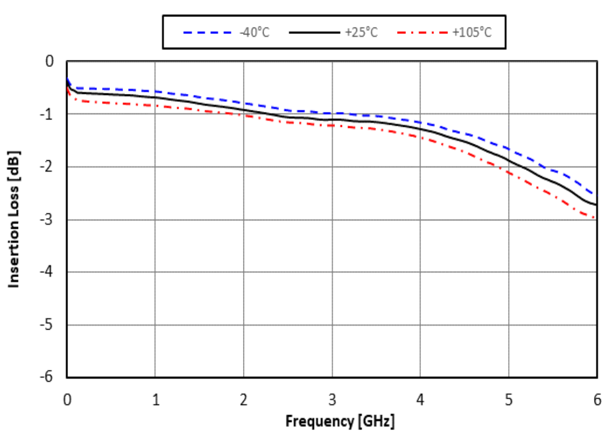
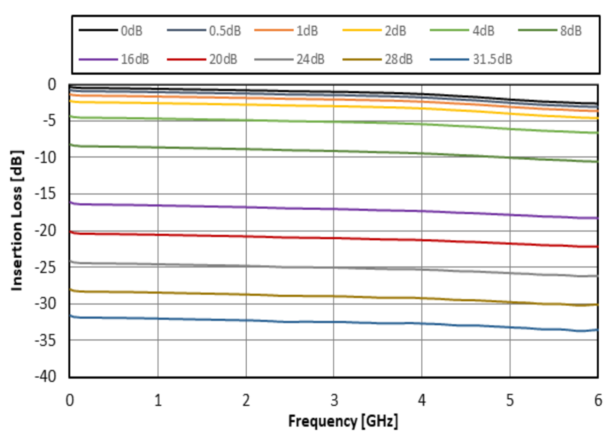


Figure 9. Insertion Loss vs ATT Setting



Typical RF Performance Plot - BDA4620 EVK - PCB (Typical Application Circuits)

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 10. Input Return Loss vs ATT Setting

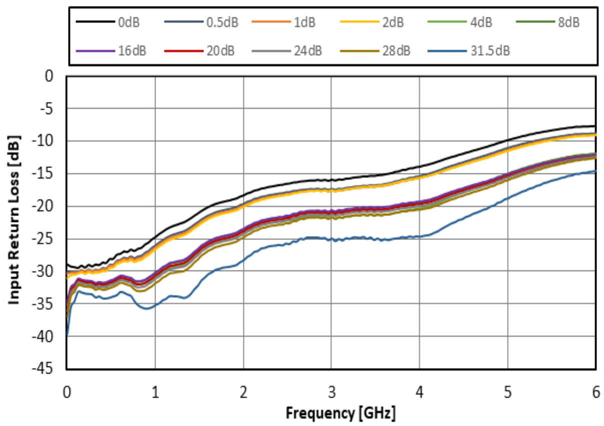


Figure 11. Output Return Loss vs ATT Setting

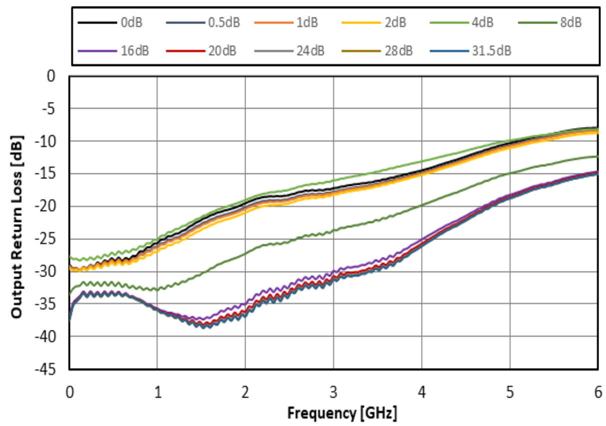


Figure 12. Input Return Loss vs Temp. @ ATT = 16dB

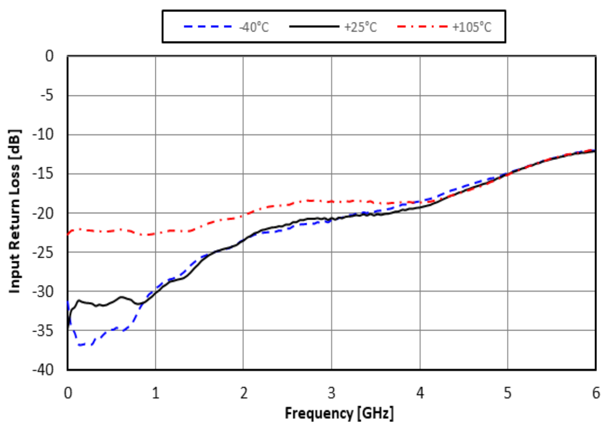


Figure 13. Output Return Loss vs Temp. @ ATT = 16dB

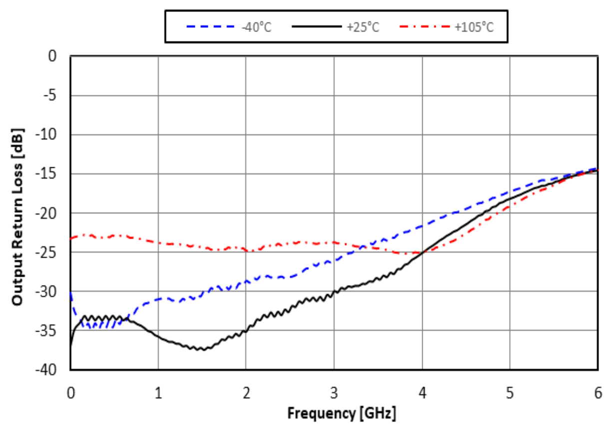


Figure 14. Relative Phase Error vs ATT Setting

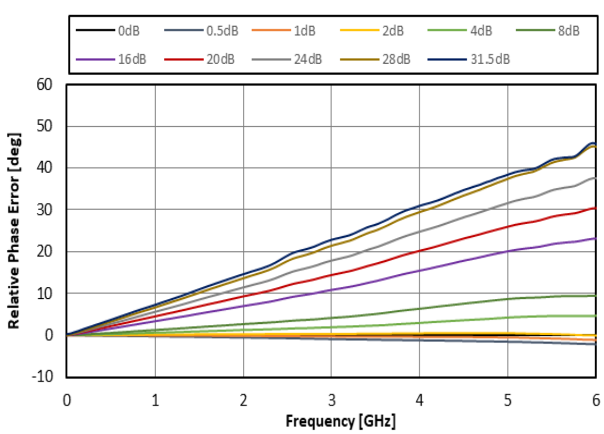
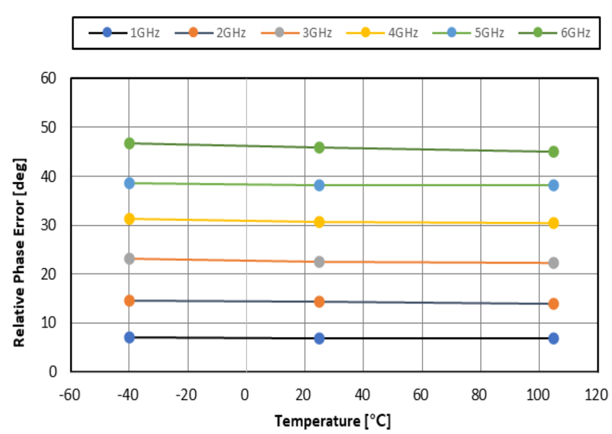


Figure 15. Relative Phase Error vs Frequency @ ATT = 31.5dB



Typical RF Performance Plot - BDA4620 EVK - PCB (Typical Application Circuits)

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 16. ATT Error vs Temp. @ 900MHz

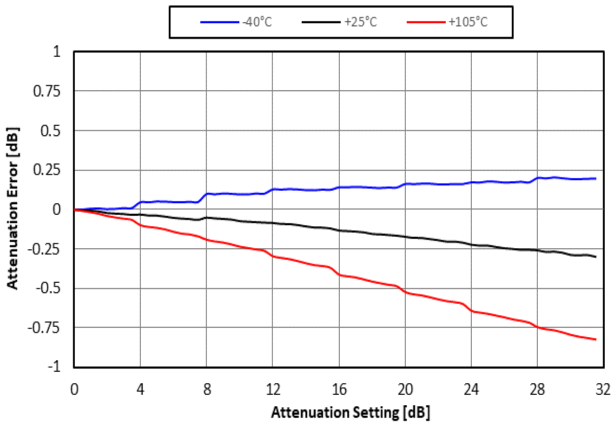


Figure 17. ATT Error vs Temp. @ 1800MHz

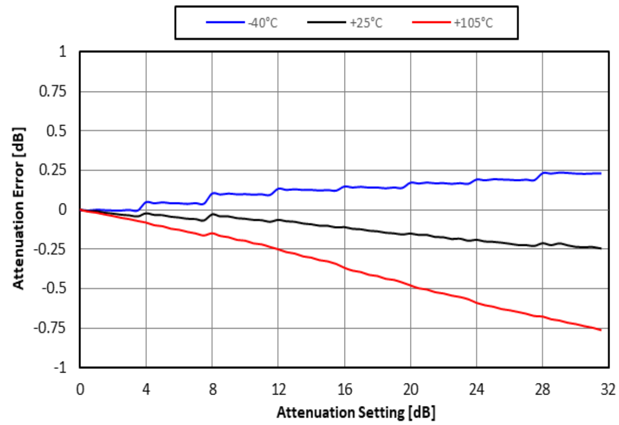


Figure 18. ATT Error vs Temp. @ 2200MHz

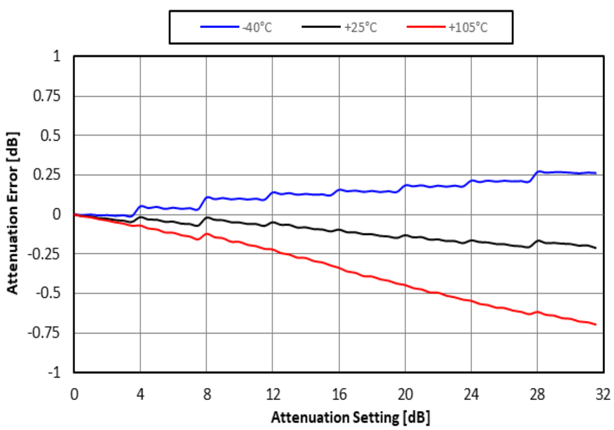


Figure 19. ATT Error vs Temp. @ 3500MHz

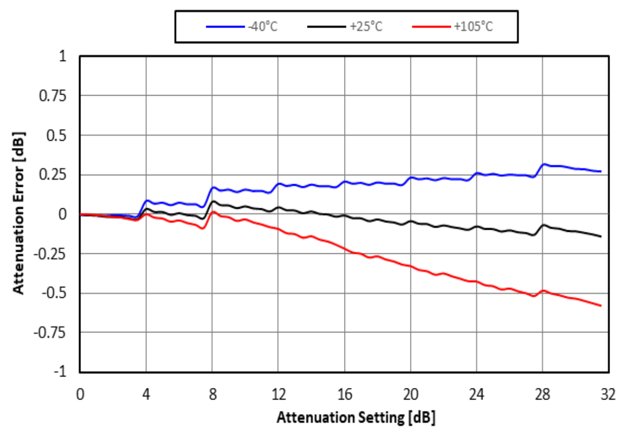


Figure 20. ATT Error vs Temp. @ 4600MHz

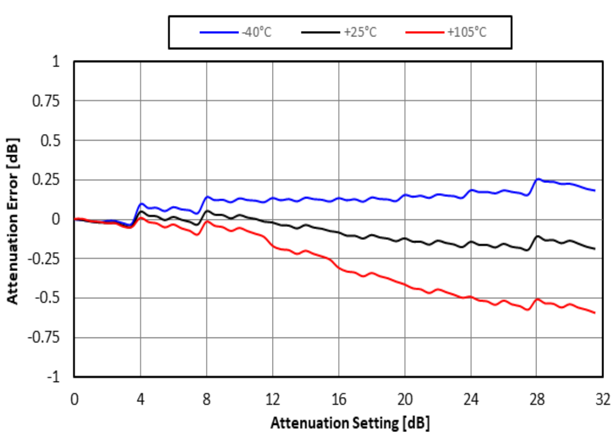
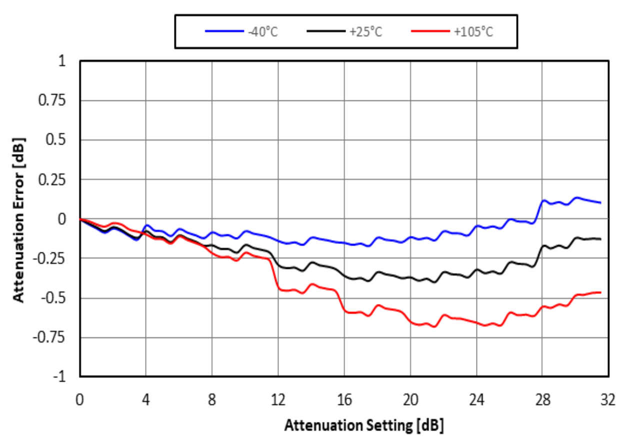


Figure 21. ATT Error vs Temp. @ 5800MHz



Typical RF Performance Plot - BDA4620 EVK - PCB (Typical Application Circuits)

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 22. IIP3 vs Temp. @ 2500MHz

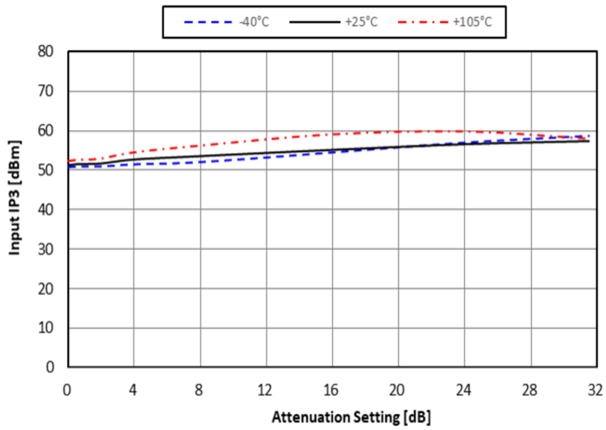


Figure 23. IIP3 vs Temp. @ 3500MHz

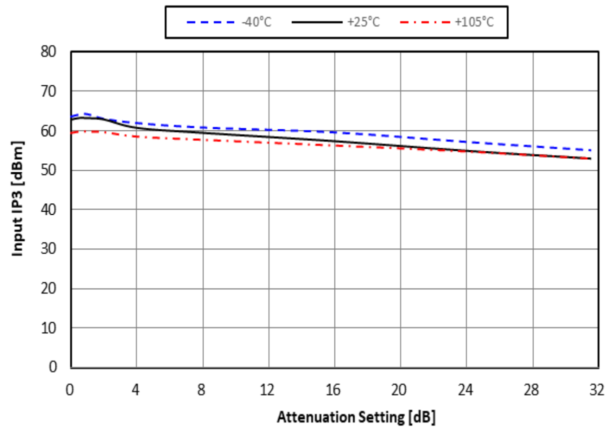


Figure 24. IIP3 vs Temp. @ 4500MHz

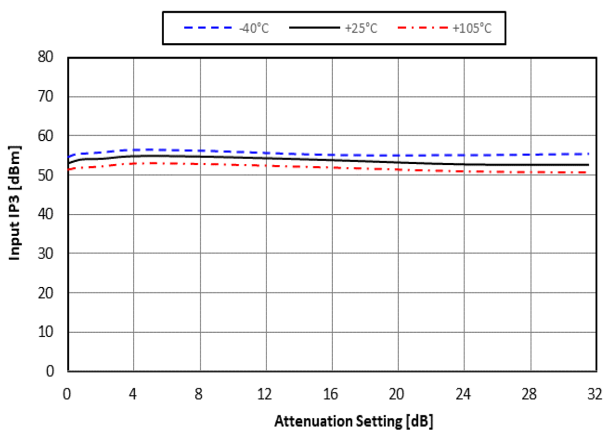


Figure 25. Input 0.1dB Compression vs Temp. @ 2500MHz

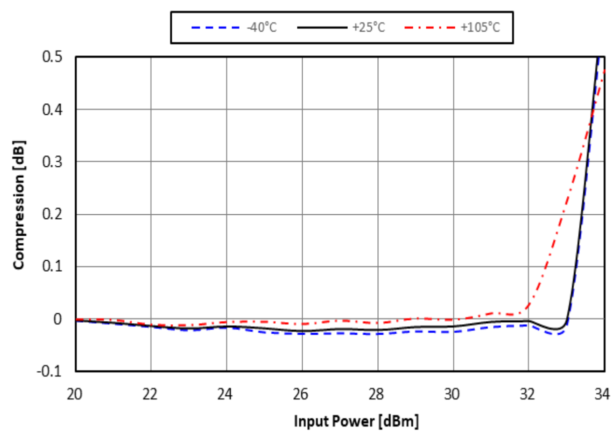


Figure 26. Input 0.1dB Compression vs Temp. @ 3500MHz

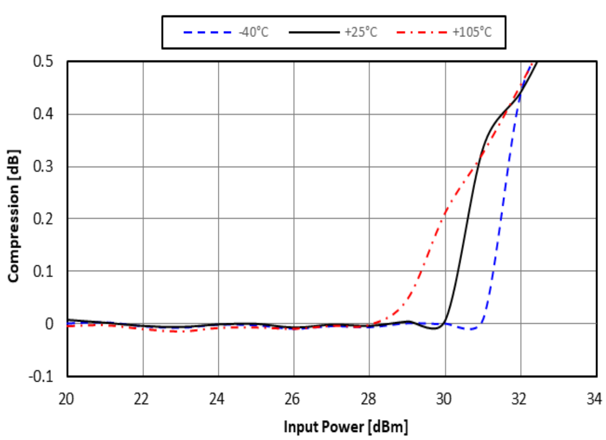
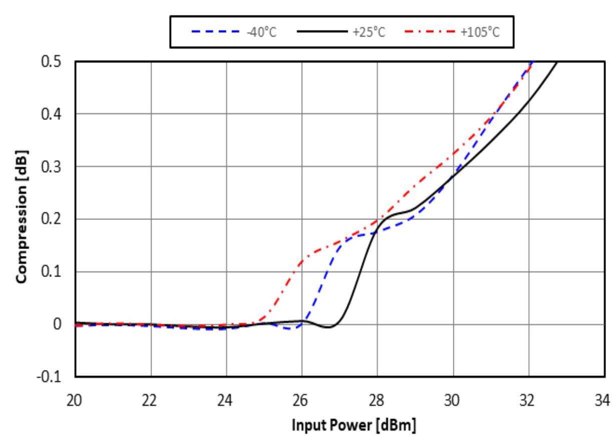


Figure 27. Input 0.1dB Compression vs Temp. @ 4500MHz



Typical RF Performance Plot - BDA4620 EVK - PCB (Typical Application Circuits)

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 28. 0.5dB Step ATT vs Frequency

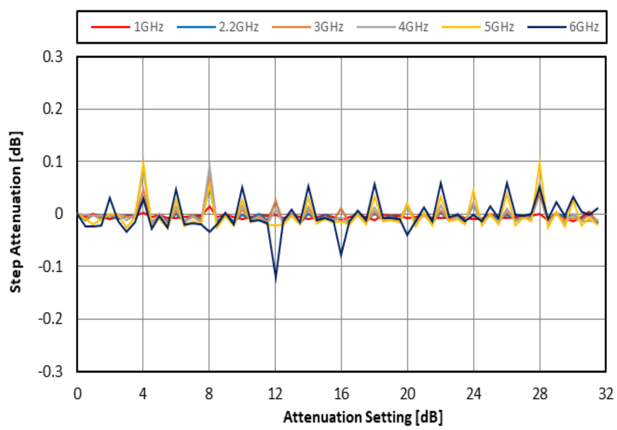


Figure 29. 0.5dB Step ATT Actual vs Frequency

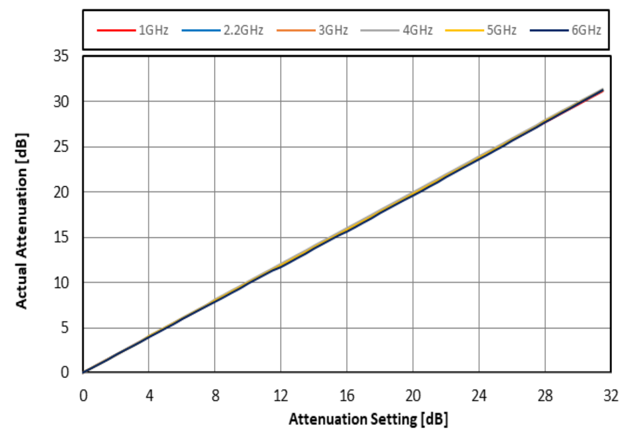


Figure 30. Major State Bit Error vs ATT Setting

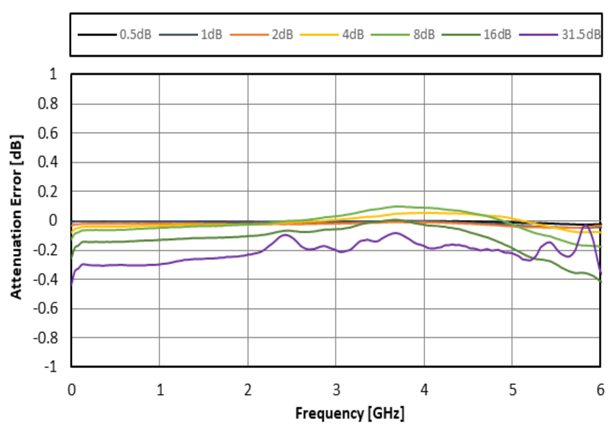


Figure 31. 0.5dB Step ATT Error vs Frequency

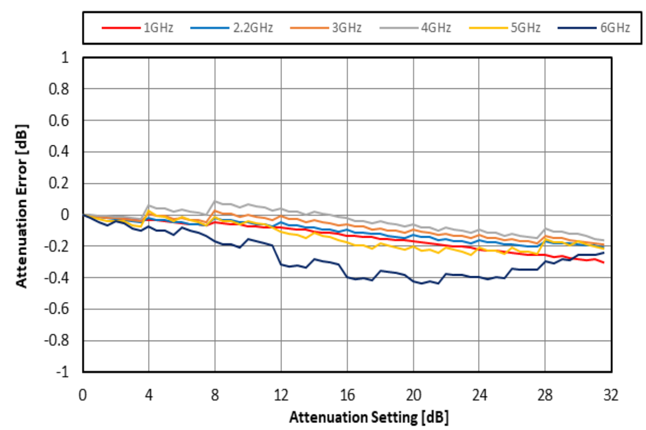


Figure 32. ATT Transient (15.5 to 16dB, Pin=18dBm)

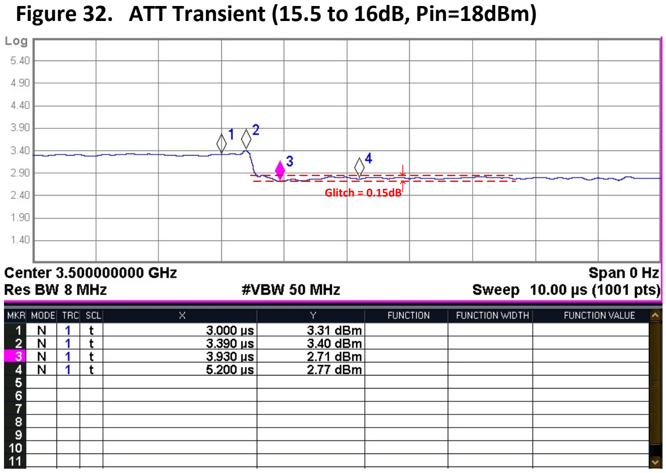
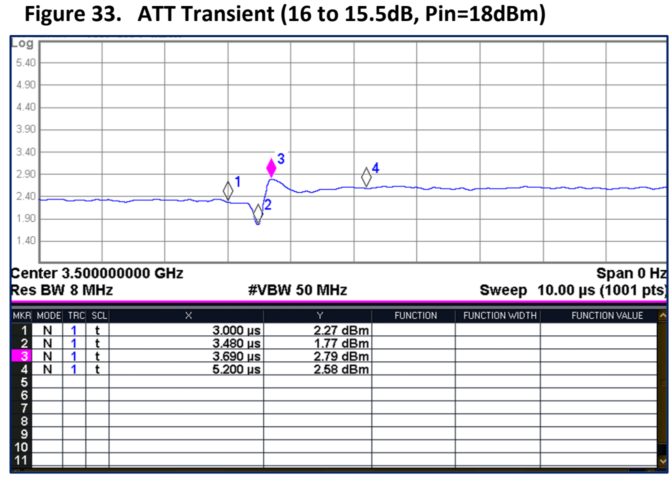


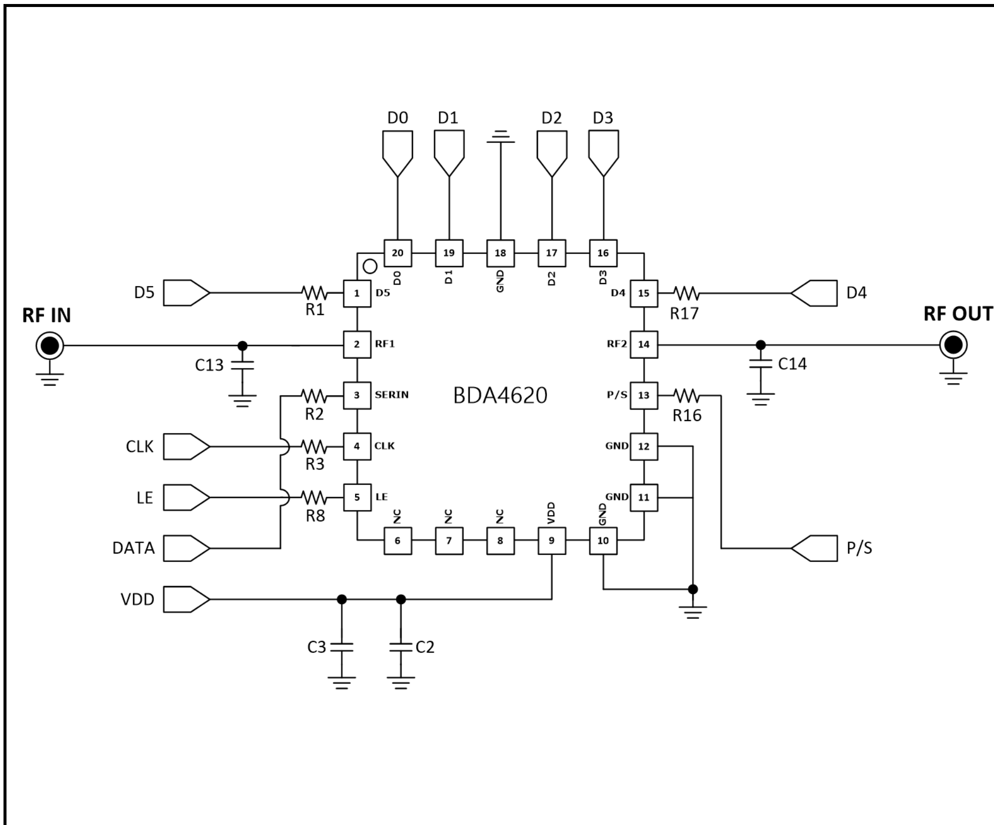
Figure 33. ATT Transient (16 to 15.5dB, Pin=18dBm)



Typical RF Performance Plot - BDA4620 EVK - PCB (Optimized Return Loss Application Circuits)

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Table 13. Optimized Return Loss Application Circuits for 4GHz - 8GHz



BOM	
C2	100pF
C3	100nF
C13,C14	0.1pF
R1-R3,R8,R16,R17	1kohm

1. See the page 18 the Evaluation Board Circuits for the detailed application circuit information.
2. In order to optimized Return loss for above 4GHz, shunt capacitor 0.1pF was added near RF1 & RF2, respectively.

Figure 34. Insertion Loss vs Temp.

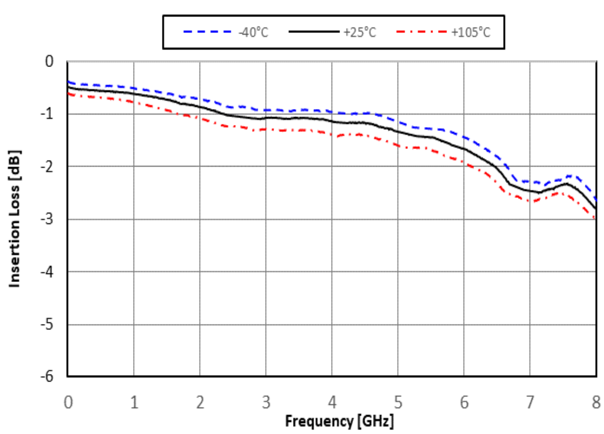
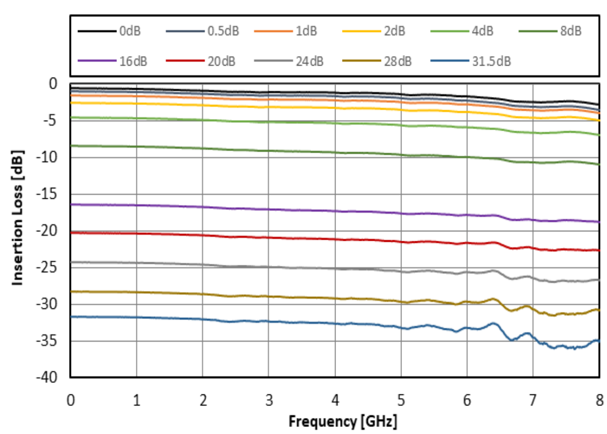


Figure 35. Insertion Loss vs ATT Setting



Typical RF Performance Plot - BDA4620 EVK - PCB (Optimized Return Loss Application Circuits)

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 36. Input Return Loss vs ATT Setting

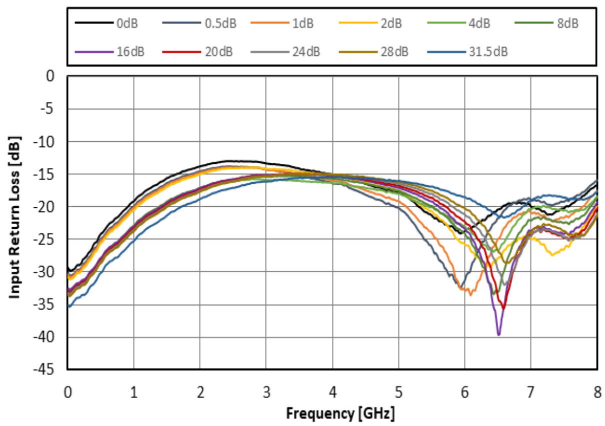


Figure 37. Output Return Loss vs ATT Setting

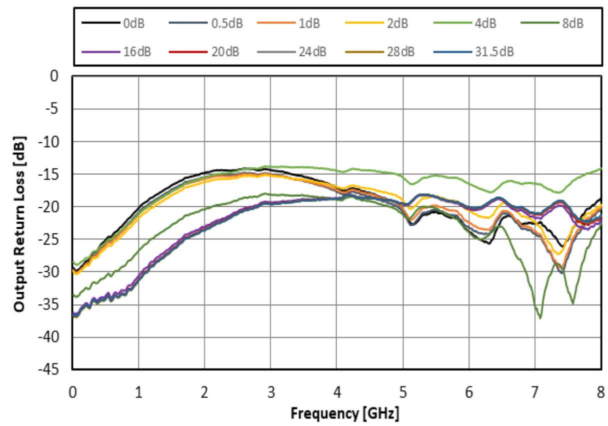


Figure 38. Input Return Loss vs Temp. @ ATT = 0dB

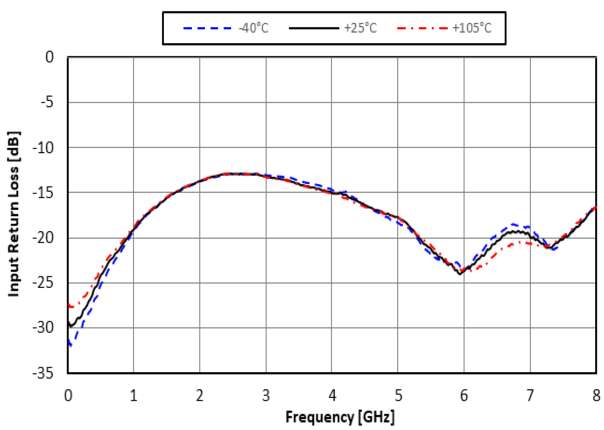


Figure 39. Output Return Loss vs Temp. @ ATT = 0dB

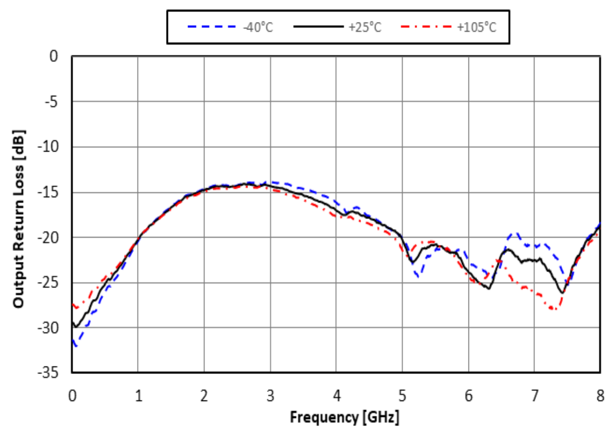


Figure 40. Relative Phase Error vs ATT Setting

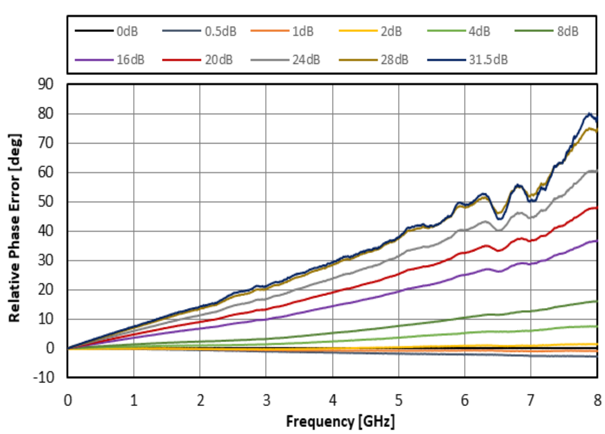
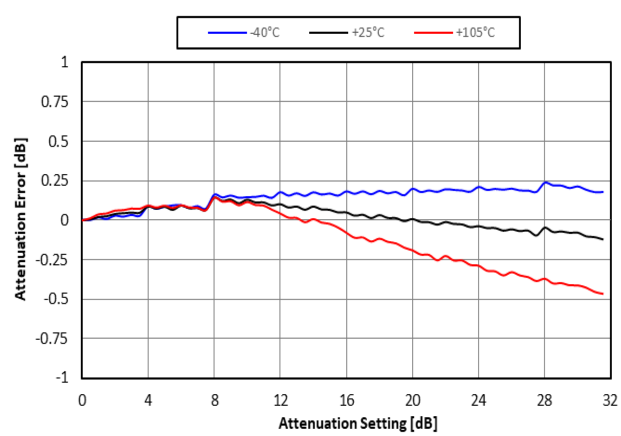


Figure 41. ATT Error vs Temp. @ 3500MHz



Typical RF Performance Plot - BDA4620 EVK - PCB (Optimized Return Loss Application Circuits)

Typical Performance Data @ 25°C and V_{DD} = 3.3V, EVKit RF connector and board losses are de-embedded, unless otherwise noted

Figure 42. ATT Error vs Temp. @ 4600MHz

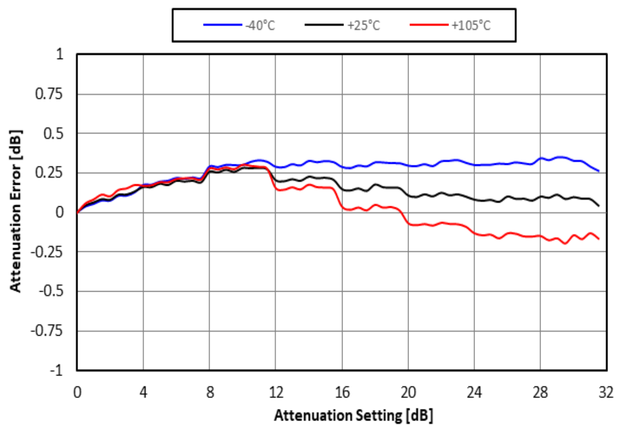


Figure 43. ATT Error vs Temp. @ 5800MHz

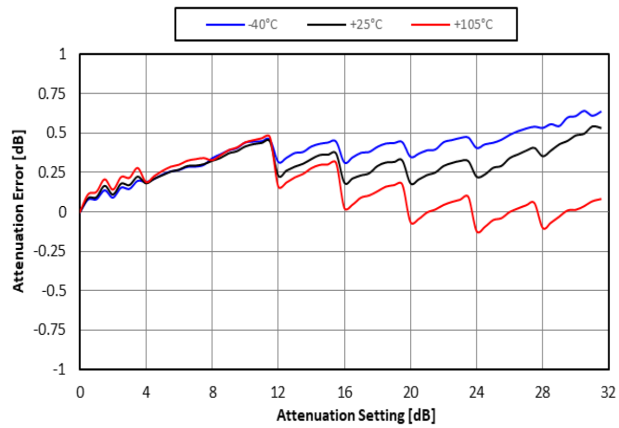


Figure 44. ATT Error vs Temp. @ 7200MHz

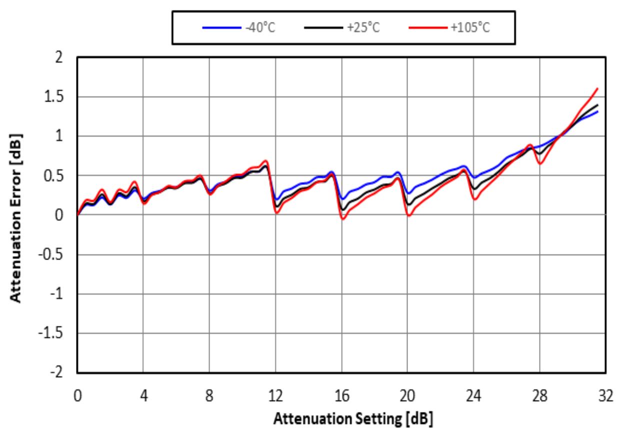


Figure 45. 0.5dB Step Actual ATT vs Frequency

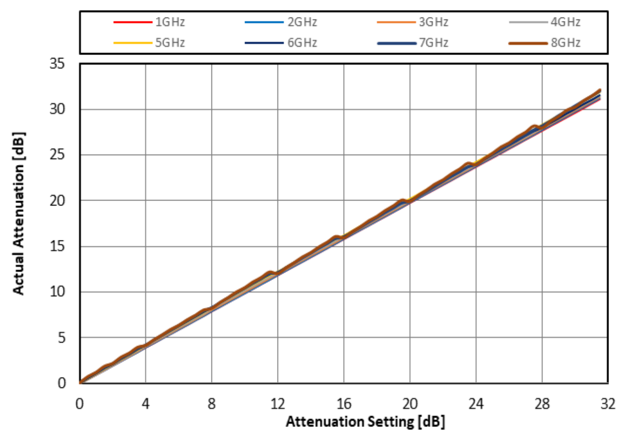


Figure 46. Major State Bit Error vs ATT Setting

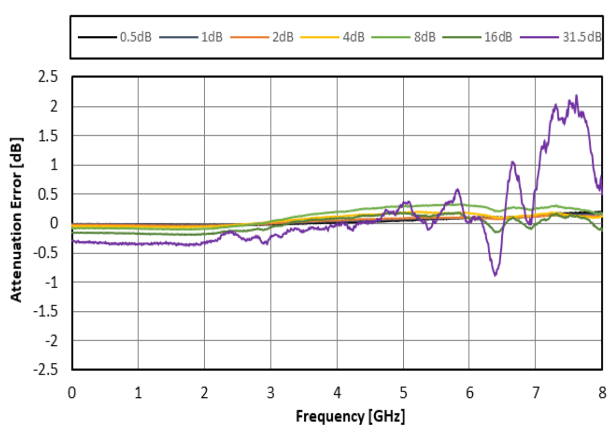
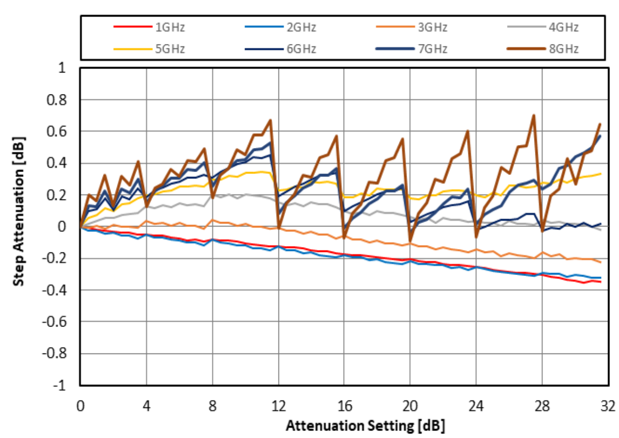


Figure 47. 0.5dB Step ATT Error vs Frequency



BDA4620 Evaluation board Kit Description

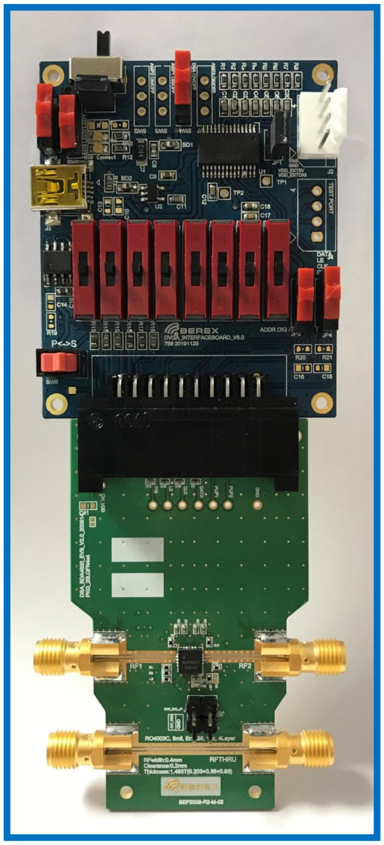


Figure 48. BDA4620 EVK

Evaluation board Kit Introduction

BDA4620 Evaluation Kit is made up of a combination of an RF board and an interface board

The schematic of the BDA4620 evaluation RF board is shown in Figure 48. The BDA4620 evaluation RF board is constructed of a 4-layer material with a copper thickness of 0.7 mils on each layer. Every copper layer is separated with a dielectric material. The top dielectric material is 8 mils RO4003. The middle and bottom dielectric materials are FR-4, used for mechanical strength and overall board thickness of approximately 1.63mm.
BDA4620 Evaluation INTERFACE board is assembled with a SP3T switches(D0~D5,LE), SP2T mechanical switch (P/S), and several header & switch.

Evaluation Board Programming Using USB Interface

In order to evaluate the BDA4620 performance, the Application Software has to be installed on your computer. And The DSA application software GUI supports Latched Parallel and Serial modes. software can be downloaded from BeRex's website

Serial Control Mode

- Connect directly the Evaluation INTEFRACE board USB port(J3) to PC
- Set the direction of P<->S Switch to S direction (P/S Logic HIGH)
- Set the D0~D5, LE switch to the middle position.
- Operate the 0~31.5dB attenuation state in GUI and then control the DSA

Latched Parallel Control Mode

- Connect directly the Evaluation INTEFRACE board USB port(J3) to PC
- Set the direction of P<->S Switch to P direction (P/S Logic LOW)
- Set the D0~D5, LE switch to the middle position.
- Operate the 0~31.5dB attenuation state in GUI and then control the DSA

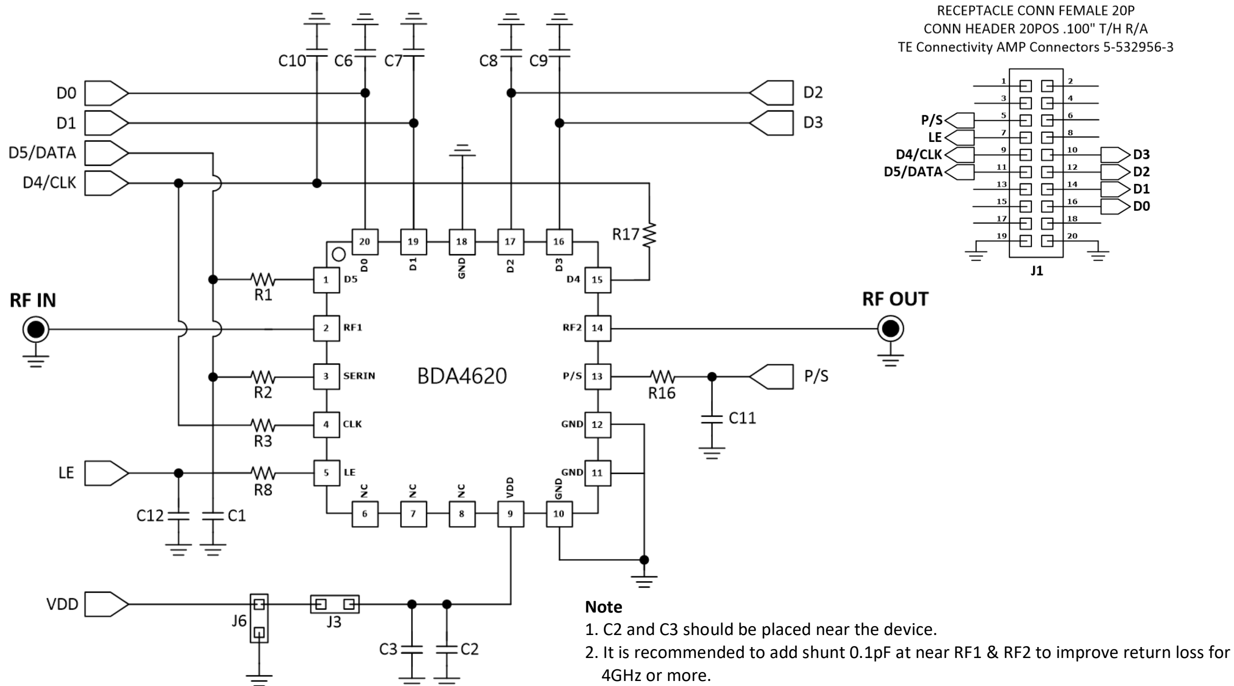
Direct Parallel Control Mode

- Set the direction of P<->S Switch to P direction (P/S Logic LOW)
- Set LE switch to the LOW Position
- For the setting to attenuation state, D0~D5 switches can be combined in manually program, refer to Table 10.

Please refer to user manual for more detailed operation method of BDA4620 EVK.

BDA4620 Evaluation board Kit Description

Figure 49. Evaluation Board Kit Schematic Diagram



Note
1. C2 and C3 should be placed near the device.
2. It is recommended to add shunt 0.1pF at near RF1 & RF2 to improve return loss for 4GHz or more.

Figure 50. Evaluation Board PCB Layout Information

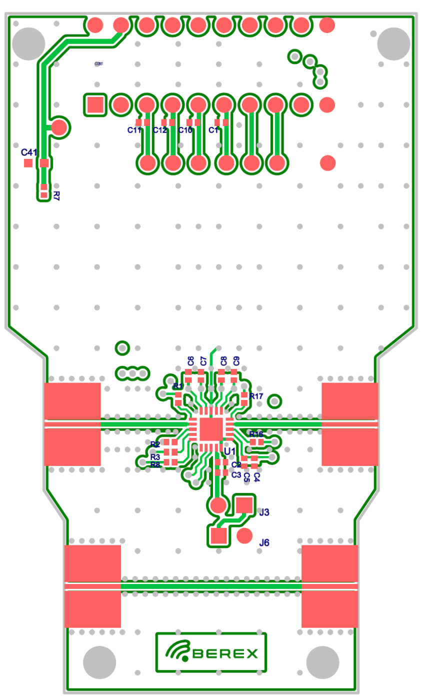


Table 14. Bill of Material - Evaluation Board

No.	Ref Des	Part Qty	Value	Description	Remark
1	C2	1	100pF	CAP, 0402, CHIP Ceramic, ±0.25%	
2	C3	1	100nF	CAP, 0402, CHIP Ceramic, ±0.25%	
3	R1,R2,R3,R8,R16,R17	6	1k ohm	RES, 0402, CHIP, ±5%	
4	U1	1	Chip	DSA, BDA4620 QFN4x4 20L	
5	SMA1, SMA2	2	CON	SMA END LAUNCH	
6	J1	1	CON	Receptacle connector 20pin	
7	J3, J6	2	CON	Header 2.54mm 2pin	
8	R7,C1,C4-C12,C41	12	NC	Not Connected	

Figure 51. Evaluation Board PCB Layer Information

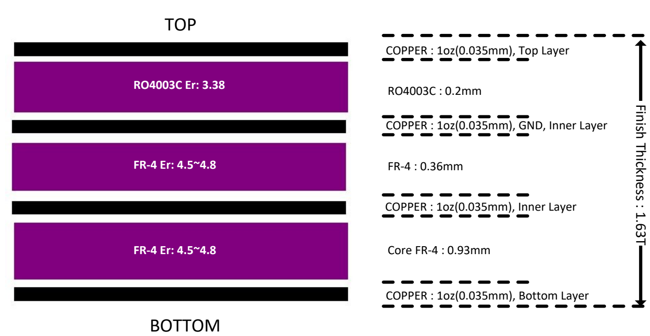
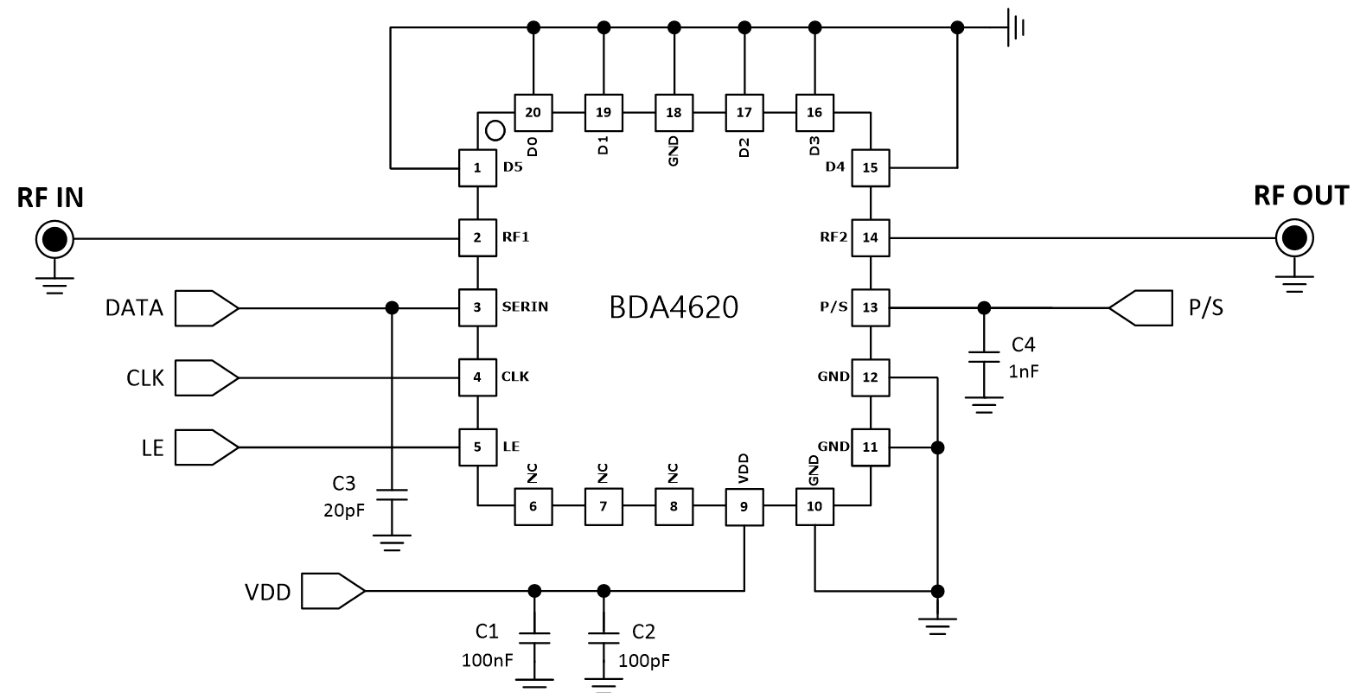
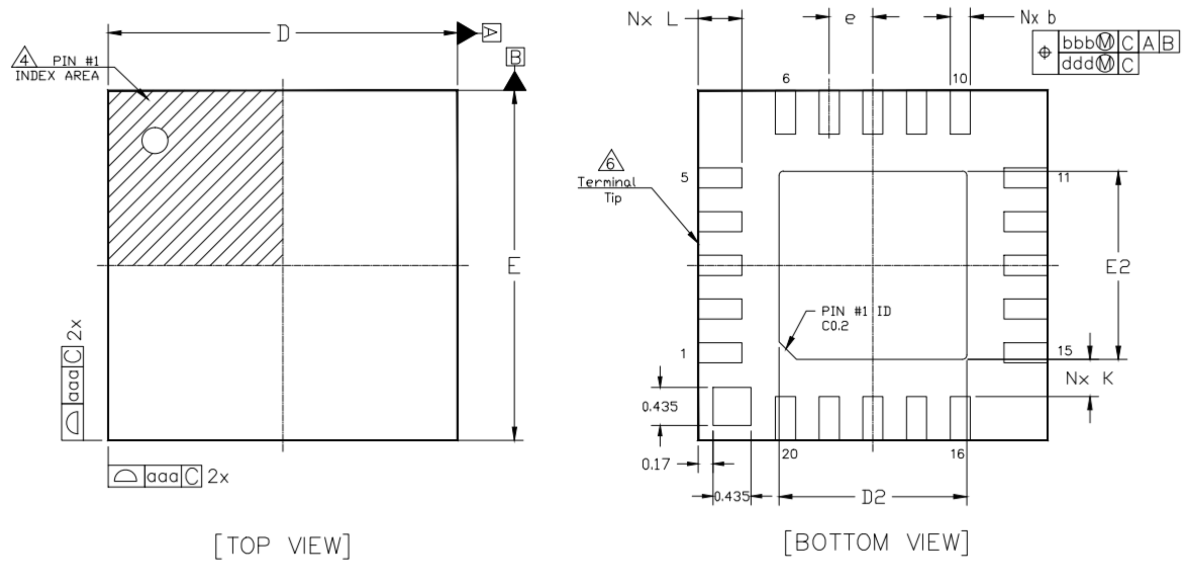


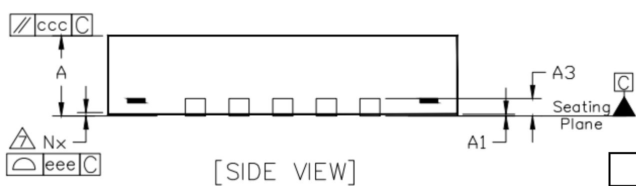
Figure 52. Recommended Serial mode Application Circuit Schematic



Note: 1. C1~C4 should be placed near the device.
2. LE pin should be pulled down.

Figure 53. **Packing Outline Dimension**





NOTE :
1. Dimensioning and tolerancing conform to ASME Y14.5-2009.

2. All dimensions are in millimeters.

3. N is the total number of terminals.

4. The location of the marked terminal #1 identifier is within the hatched area.

5. ND and NE refer to the number of terminals on each D and E side respectively.

6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.

7. Coplanarity applies to the terminals and all other bottom surface metallization

Dimension Table				
Symbol	Thickness			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	–––	0.203 Ref	–––	
b	0.18	0.23	0.28	6
D		4.00 BSC		
E		4.00 BSC		
e		0.50 BSC		
D2	2.10	2.15	2.20	
E2	2.10	2.15	2.20	
K	0.20	–––	–––	
L	0.45	0.55	0.65	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		20		3
ND		5		5
NE		5		5

Figure 54. Recommend Land Pattern

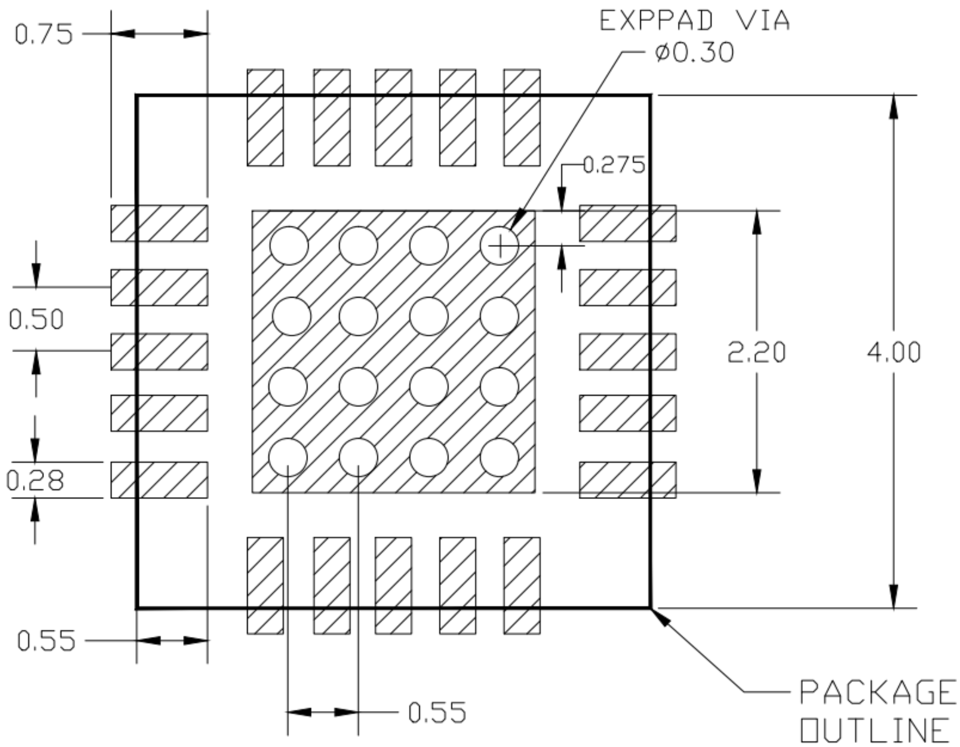
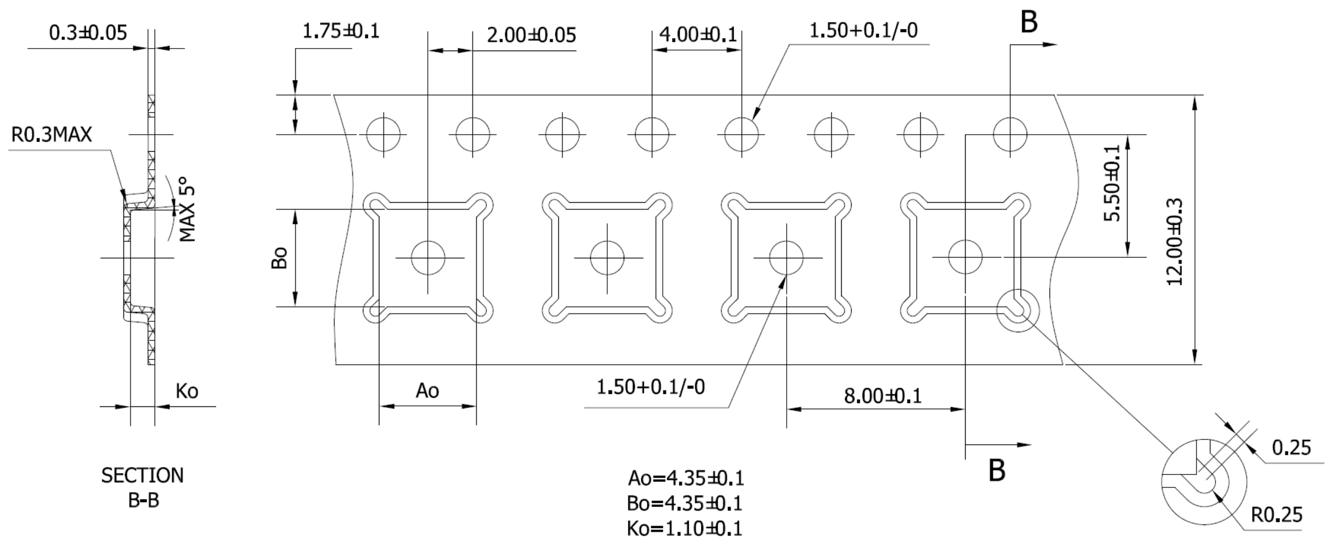


Figure 55. Package Marking

Marking information:	
BDA4620	Device Name
YY	Year
WW	Work Week
XX	LOT Number

Figure 56. Tape & Reel



NOTES:
1 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2 CAMBER IN COMPLANCE WITH EIA 481
3 POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED
AS TRUE POSITION OF POCKET,NOT POCKET HOLE

Packaging information:	
Tape Width	12mm
Reel Size	7inch
Device Cavity Pitch	8mm
Devices Per Reel	1k

Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	Class 1C
Value:	±1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JS-001-2017
ESD Rating:	Class C3
Value:	±1000V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JS-002-2018
MSL Rating:	**Level 1 at +260°C convection reflow**
Standard:	JEDEC Standard J-STD-020

Caution: ESD Sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

2	**N**	**9**	**6**	**F**