BVA1621

High Linearity wideband DVGA with addressable function

400MHz - 4000MHz

Preliminary Datasheet

Device Features

- Integrate DSA to AMP Functionality
- 400 - 4000MHz Broadband Performance
- Wide Supply Voltage Range
  AMP : 3.3V to 5.25V
  DSA : 2.7V to 5.5V
- Low current : 85mA @ 5V, 48mA @ 3.3V
- High Gain
  20dB@800MHz, 17.8dB@2.7GHz (VDD=5V)
  19.5dB@800MHz, 17.3dB@2.7GHz (VDD=3.3V)
- High OP1dB
  21dBm@800MHz, 20.5dBm@2.7GHz (VDD=5V)
  18.5dBm@800MHz, 17.5dBm@2.7GHz (VDD=3.3V)
- High OIP3
  37.5dBm@800MHz, 36.8dBm@2.7GHz (VDD=5V)
  33dBm@800MHz, 32.5dBm@2.7GHz (VDD=3.3V)
- Noise Figure at max gain setting
  1.9dB@800MHz, 2.3dB@2.7GHz (VDD=5V)
- Attenuation Range : Up to 31.5dB / 0.5dB step
- Safe attenuation state transitions
- Excellent attenuation accuracy
  ±(0.15 + 3% x ATT) @ 800MHz
  ±(0.25 + 3% x ATT) @ 2.7GHz
- Programming modes
  Serial mode with Addressable function
  Latched Parallel Mode
  Direct Parallel Mode
- 3bit Addressable function
  LE/DATA/CLK can be shared up to 8EA Chips
- Lead-free/RoHS2-compliant 32-lead 5mm x 5mm x 1.07mm SIP LGA SMT package

32-lead 5mm x 5mm x 1.07mm SIP LGA

Figure 1. Package Type

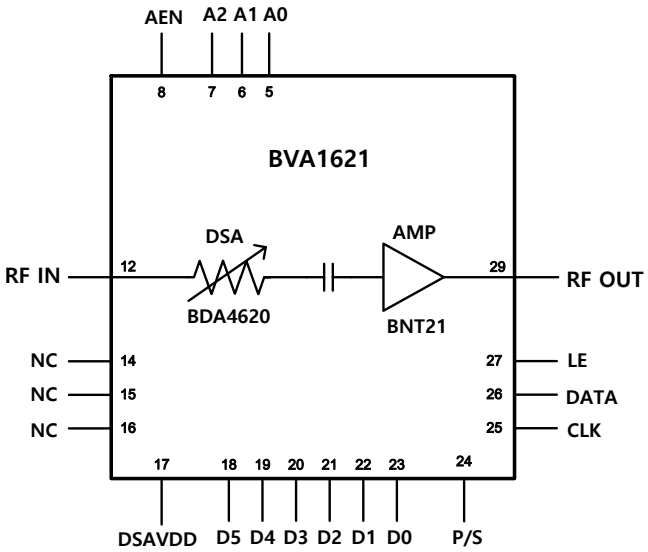


Figure 2. Functional Block Diagram

Product Description

The BVA1621 is a high performance, digitally controlled variable gain amplifier (DVGA) operating from 400MHz to 4GHz.

The BVA1621 integrates a high performance digital step attenuator (DSA) and a high linearity, broadband gain block amplifier operating voltage 3.3V to 5.25V DC within enable control using the small package.

Both DSA and gain block amplifier in BVA1621 are internally matched to 50 ohms and It is easy to use with minimum external matching components required.

The BVA1621 can control 6bit attenuation to 0.5dB step up to 31.5dB and initialize to the maximum attenuation setting on power-up until next programming word is inputted.

In addition, Internal DSA has a 3-bit addressable function, so it can share up to 8 DSAs(or DVGAs) Latch Enable(LE), DATA(SERIN) and CLOCK(CLK) pin. This has the advantage of reducing the number of IO pins when using multiple DSA or DVGA chip with addressable function.

The BVA1621 is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless application.

Application

- 5G/4G/3G Wireless infrastructure and other high performance RF application
- Microwave and Satellite Radio
- General purpose Wireless

Table 1. Electrical Specifications[1] @ VDD = 5V

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			400		4000	MHz
Gain [2]		ATT = 0dB @ 800MHz		20		dB
		ATT = 0dB @ 1.8GHz		18.7		
		ATT = 0dB @ 2.7GHz		17.8		
		ATT = 0dB @ 3.5GHz		17		
Attenuation Control range		0.5dB Step		0 - 31.5		dB
Attenuation Step				0.5		dB
Attenuation Accuracy	400MHz - 1GHz	Any bit or bit combination			±(0.15 + 3% of ATT setting)	dB
	1GHz - 2GHz				±(0.25 + 3% of ATT setting)	
	2GHz - 3GHz				±(0.25 + 3% of ATT setting)	
	3GHz - 4GHz				±(0.25 + 5% of ATT setting)	
Input Return loss	400MHz - 2GHz	ATT = 0dB		-13		dB
	2GHz - 4GHz			-13		
Output Return loss	400MHz - 2GHz	ATT = 0dB		-13		dB
	2GHz - 4GHz			-13		
Output Power for 1dB Compression		ATT = 0dB @ 800MHz		21		dBm
		ATT = 0dB @ 1.8GHz		20.9		
		ATT = 0dB @ 2.7GHz		20.5		
		ATT = 0dB @ 3.5GHz		20		
Output Third Order Intercept Point [3]		ATT = 0dB @ 800MHz		37.5		dBm
		ATT = 0dB @ 1.8GHz		37		
		ATT = 0dB @ 2.7GHz		36.8		
		ATT = 0dB @ 3.5GHz		36.5		
Noise Figure		ATT = 0dB @ 800MHz		1.9		dB
		ATT = 0dB @ 1.8GHz		2.2		
		ATT = 0dB @ 2.7GHz		2.3		
		ATT = 0dB @ 3.5GHz		3		
DSA Switching time		50% CTRL(LE) to 90% or 10% RF		500	800	ns
AMP Switching time		50% CTRL(AEN) to 90% or 10% RF		150		ns
Impedance				50		Ω

1. Device performance : measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+5.0V.
2. Gain data has PCB & Connectors insertion loss de-embedded.
3. OIP3 _ measured with two tones at an output of 0dBm per tone separated by 1MHz.

Table 2. Electrical Specifications[1] @ VDD = 3.3V

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			400		4000	MHz
Gain [2]		ATT = 0dB @ 800MHz		19.5		dB
		ATT = 0dB @ 1.8GHz		18.2		
		ATT = 0dB @ 2.7GHz		17.3		
		ATT = 0dB @ 3.5GHz		16.5		
Attenuation Control range		0.5dB Step		0 - 31.5		dB
Attenuation Step				0.5		dB
Attenuation Accuracy	400MHz - 1GHz	Any bit or bit combination			±(0.15 + 3% of ATT setting)	dB
	1GHz - 2GHz				±(0.25 + 3% of ATT setting)	
	2GHz - 3GHz				±(0.25 + 3% of ATT setting)	
	3GHz - 4GHz				±(0.25 + 5% of ATT setting)	
Input Return loss	400MHz - 2GHz	ATT = 0dB		-13		dB
	2GHz - 4GHz			-13		
Output Return loss	400MHz - 2GHz	ATT = 0dB		-13		dB
	2GHz - 4GHz			-13		
Output Power for 1dB Compression		ATT = 0dB @ 800MHz		18.5		dBm
		ATT = 0dB @ 1.8GHz		18		
		ATT = 0dB @ 2.7GHz		17.5		
		ATT = 0dB @ 3.5GHz		16.5		
Output Third Order Intercept Point [3]		ATT = 0dB @ 800MHz		33		dBm
		ATT = 0dB @ 1.8GHz		33		
		ATT = 0dB @ 2.7GHz		32.5		
		ATT = 0dB @ 3.5GHz		32		
Noise Figure		ATT = 0dB @ 800MHz		2		dB
		ATT = 0dB @ 1.8GHz		2.3		
		ATT = 0dB @ 2.7GHz		2.5		
		ATT = 0dB @ 3.5GHz		3		
DSA Switching time		50% CTRL(LE) to 90% or 10% RF		500	800	ns
AMP Switching time		50% CTRL(AEN) to 90% or 10% RF		150		ns
Impedance				50		Ω

1. Device performance : measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+3.3V.
2. Gain data has PCB & Connectors insertion loss de-embedded.
3. OIP3 _ measured with two tones at an output of 0dBm per tone separated by 1MHz.

Table 3. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage	AMP			5.5	V
	DSA			5.5	V
Supply Current	AMP			190	mA
	DSA			1000	uA
Digital input voltage	AMP Control Pin (AEN)	-0.3		5.25	V
	DSA Control Pin (LE, DATA, CLK, P/S, D0 - D5, A0, A1, A2)	-0.3		3.6	V
Maximum input power	AMP			20	dBm
	DSA			30	dBm
Storage Temperature		-55		150	℃
Junction Temperature			150		℃

Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	DSA + AMP	400		4000	MHz
Supply Voltage, VDD	AMP VDD	3.3	5	5.25	V
	DSA VDD	2.7		5.5	V
Current, IDD	AMP ON @ VDD=5V		85		mA
	AMP ON @ VDD=3.3V		48		mA
	AMP OFF			7	mA
	DSA		200		uA
AEN Control Voltage	AMP ON	0		0.6	V
	AMP OFF	1.17		VDD	V
AEN pin Current	AMP OFF		150		uA
DSA Control Voltage	Digital Input High	1.17		3.6	V
	Digital Input Low	-0.3		0.6	V
DSA Control pin Current	Digital Input High			20	uA
Operating Temperature	DSA + AMP	-40		105	℃

Specifications are not guaranteed over all recommended operating conditions.

Figure 3. Pin Configuration (Top View)

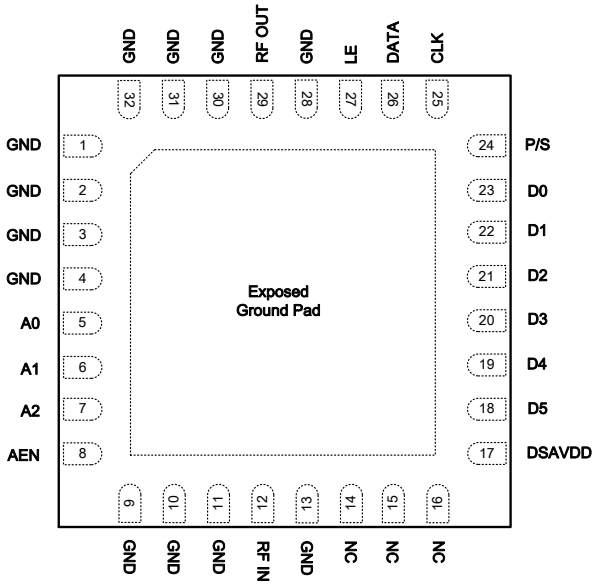


Table 5. Pin Description

Pin	Pin name	Description
5	A0	Address bit A0 connection
6	A1	Address bit A1 connection
7	A2	Address bit A2 connection
8	AEN	Amplifier(AMP) Enable / Disable Control (0 = AMP Enable, 1 = AMP Disable)
12	RF IN	RF Input (DSA RF Input)
17	DSAVDD	DSA Supply Voltage (2.7V to 5.5V)
18	D5	DSA Attenuation 16dB Control Word : MSB
19	D4	DSA Attenuation 8dB Control Word
20	D3	DSA Attenuation 4dB Control Word
21	D2	DSA Attenuation 2dB Control Word
22	D1	DSA Attenuation 1dB Control Word
23	D0	DSA Attenuation 0.5dB Control Word : LSB
24	P/S	DSA Control Mode Selection (1 = Serial Mode, 0 = Parallel Mode)
25	CLK	SPI Clock Input
26	DATA	SPI Data Input
27	LE	Latch Enable
29	RF OUT	RF Output (AMP RF Output and Supply Voltage : 3.3V to 5.25V)
14, 15, 16	NC	Not Connected
Others	GND	Ground, These pins must be connected to ground

Programming Options

BVA1621 can be programmed using either the parallel or serial interface, which is selectable via P/S pin(Pin24).

Serial mode is selected by pulling it to a voltage logic HIGH and parallel mode is selected by setting P/S to logic LOW.

Serial Control Mode

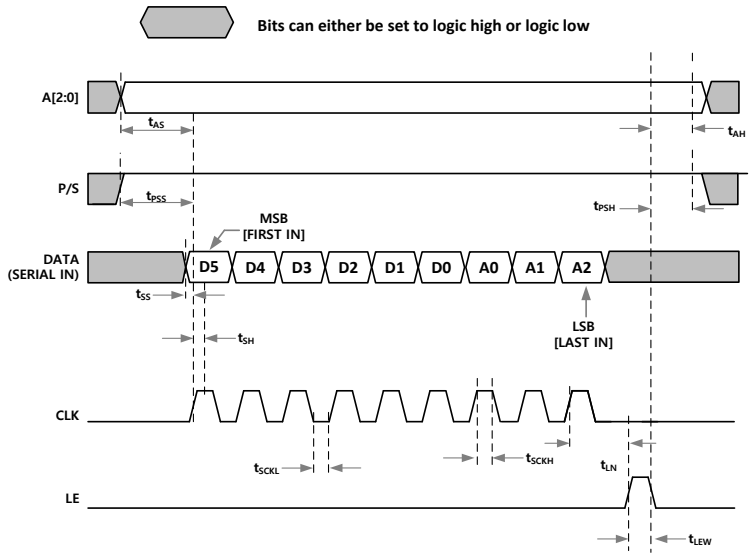
The serial interface is a 9-bit shift register to shift in the data MSB (D5) first. When serial programming is used, It is recommended all the parallel control input pins (18, 19, 20, 21, 22, 23) are grounded .

It is controlled by three CMOS-compatible signals: Serial In(DATA), Clock(CLK), and Latch Enable (LE).

Table 6. Truth Table for Serial Control Word

Digital Control Input						Attenuation State [dB]
D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	
0	0	0	0	0	0	0
0	0	0	0	0	1	0.5
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	1	0	0	0	4
0	1	0	0	0	0	8
1	0	0	0	0	0	16
1	1	1	1	1	1	31.5

Figure 4. Serial Mode Timing Diagram



BVA1621 Serial mode is selected by pulling it to logic HIGH. The serial interface is a 9-bits shift register made up of two words. The first 6-bits from MSB are the Attenuation word, which controls the DSA state. Followed by the next 3-bits are the address word, which uses 3 bits that must match the hard wired A0 - A2 programming in order to change the DSA state. If no external connections are made to A0 - A2 then internally they will default to 000 due to internal pull down resistors. If these 3 external preset address bits are not matched with the SPI loaded address bits, then the current attenuator state will remain unchanged. This allows up to 8 serial-controlled devices to be used on a single board, which share a common DATA, CLK and LE.

When serial programming is used, all the parallel control input pins 18, 19, 20, 21, 22, 23 can be left grounded or open.

Table 7. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{CLK}	Serial data clock frequency			10	MHz
t_{AS}	Address setup time	100			ns
t_{AH}	Address hold time	100			ns
t_{PSS}	Parallel/Serial setup time	100			ns
t_{PSH}	Parallel/Serial hold time	100			ns
t_{SCK}	Minimum serial period	70			ns
t_{SS}	Serial Data setup time	10			ns
t_{SH}	Serial Data hold time	10			ns
t_{LN}	LE setup time	10			ns
t_{LEW}	Minimum LE pulse width	30			ns

Figure 5. Multi Device Addressing Scheme using SPI

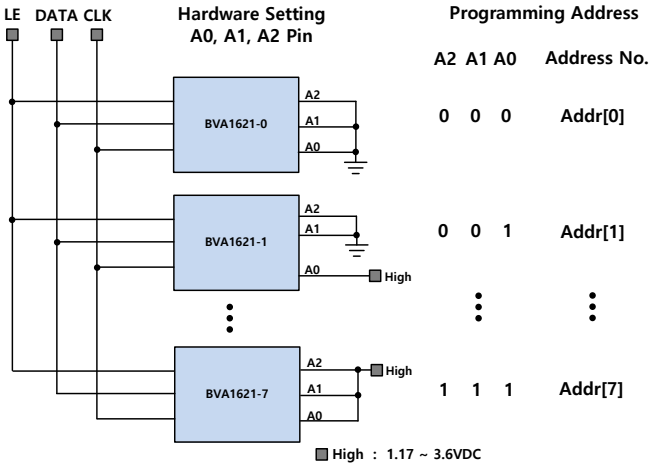


Table 8. Truth Table for Address Control Word

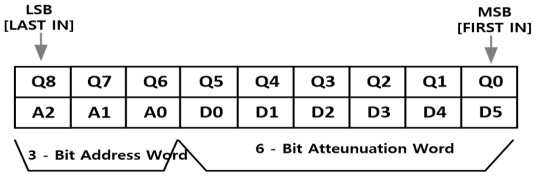
Address Digital Control Input			Address Setting	Address No.
A2	A1	A0		
0	0	0	000	Addr[0]
0	0	1	001	Addr[1]
0	1	0	010	Addr[2]
0	1	1	011	Addr[3]
1	0	0	100	Addr[4]
1	0	1	101	Addr[5]
1	1	0	110	Addr[6]
1	1	1	111	Addr[7]

Serial Register Map

The BVA1621 can be programmed via the serial control on the rising edge of Latch Enable (LE) which loads the last 6-bits attenuation word and 3-bits address word in the SHIFT Register. Data is clocked in MSB(D5) first.

The shift register must be loaded while LE is kept LOW to prevent changing the attenuation value during data is inputted.

Figure 6. Serial Register Map



The serial register consist of 9 bits as shown in Figure 6. First 6 bits from MSB are Attenuation word, 3 bits after that are Address word. The Attenuation word is DSA attenuation control bit and the Address word is static logical bit determined by A0, A1 and A2 digital inputs. The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by two because of 0.5dB step up to 31.5dB (total 63 Attenuation state), then convert to binary.

For example, to program attenuation 15.75dB state of Addr[5] BVA1621 :

Attenuation State
2 x 15.5 = 31
D0 - D5 : 111110

Address state
Digital input of A2, A1, A0 pin = 101

Serial DATA Input : 101111110

1	0	1	1	1	1	1	1	0
A2	A1	A0	D0	D1	D2	D3	D4	D5

Power-UP states Settings

The BVA1621 will always initialize to the maximum attenuation setting (31.5 dB) on power-up for both the Serial and Latched Parallel modes of operation and will remain in this setting until the user latches in the next programming word. In Direct Parallel mode, the DSA can be preset to any state within the 31.5 dB range by pre-setting the Parallel control pins prior to power-up.

Programming Options

Parallel Control Mode

The parallel control interface has seven digital control input lines (D5 to D0) to set the attenuation value. D5 is the most significant bit (MSB) that selects the 16 dB attenuator stage, and D0 is the least significant bit (LSB) that selects the 0.5 dB attenuator stage.

Direct Parallel Mode

For direct parallel mode, The LE pin must be kept HIGH. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 18, 19, 20, 21, 22, 23]. Use direct parallel mode for the fastest settling time.

Latched Parallel Mode

The LE pin must be kept LOW when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled HIGH to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled LOW to latch the change into the device until the next desired attenuation change (see Figure 7 and Table 9).

- Set P/S is logic LOW.
- Set LE to logic LOW.
- Adjust pins [18, 19, 20, 21, 22, 23] to the desired attenuation setting. (Note the device will not react to these pins while LE is a logic LOW).
- Pull LE to a logic HIGH. The device will then transition to the attenuation settings reflected by pins D5 - D0.
- If LE is pulled to a logic LOW then the attenuator will not change state.

Latched Parallel Mode implies a default state for when the device is first powered up with P/S pin set for logic LOW and LE logic LOW. In this case the default setting is **Maximum attenuation** .

Switching Feature Description

Glitch-Safe Attenuation State Transient

The BVA1621 is the latest product applied *Glitch-Safe* technology with less than 1dB ringing (positive/negative) across the attenuation range when changing attenuation states. This technology protects Amplifiers or ADC during transitions between attenuation states.

Table 9. Truth Table for the Parallel Control Word

D5	D4	D3	D2	D1	D0	P/S	LE	Attenuation State(dB)
0	0	0	0	0	0	0	1	0 (RL)
0	0	0	0	0	1	0	1	0.5
0	0	0	0	1	0	0	1	1.0
0	0	0	1	0	0	0	1	2.0
0	0	1	0	0	0	0	1	4.0
0	1	0	0	0	0	0	1	8.0
1	0	0	0	0	0	0	1	16.0
1	1	1	1	1	1	0	1	31.5

Figure 7. Latched Parallel Mode Timing Diagram

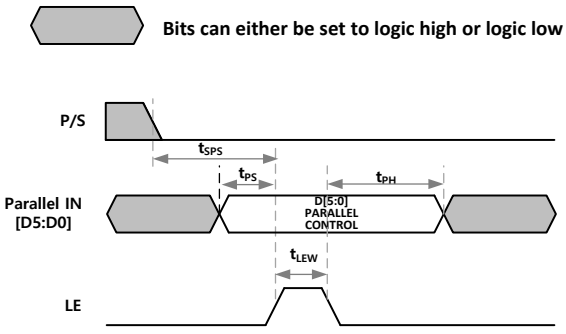


Table 10. Parallel Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_{SPS}	Serial to Parallel Mode Setup Time	100			ns
t_{LEW}	Minimum LE pulse width	10			ns
t_{PH}	Data hold time from LE	10			ns
t_{PS}	Data setup time to LE	10			ns

Figure 8. Evaluation Board Schematic Diagram

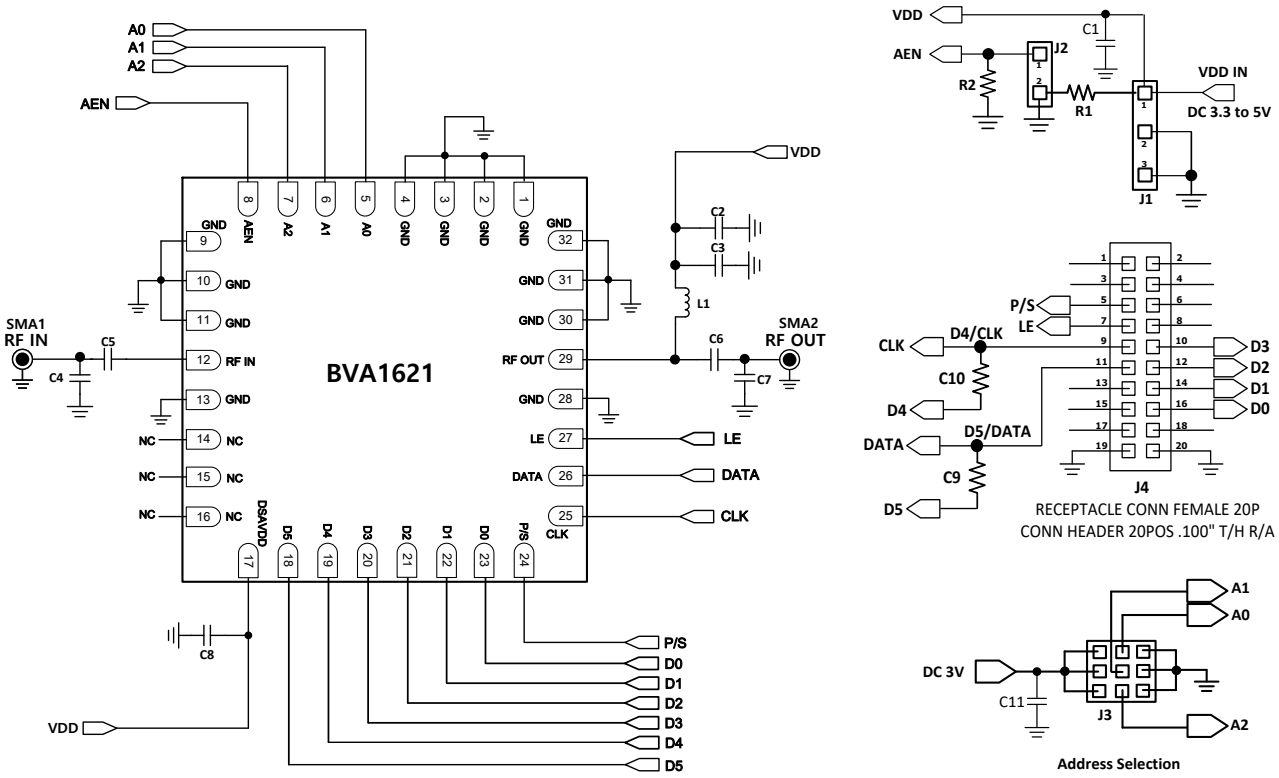
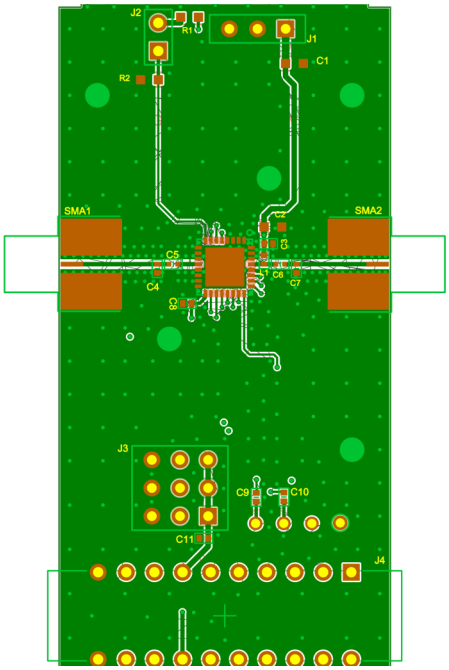


Figure 9. BVA1621 Evaluation Board



BOM (Application Circuits by Frequency Range)				
Ref. Num	**0.4 - 1.5GHz**	**1.5 - 2.7GHz**	**3 - 4GHz**	**Remark**
C1	1uF	1uF	1uF	Capacitor 0608
C2	100nF	100nF	100nF	Capacitor 0608
C3	100pF	100pF	100pF	Capacitor 0402
C5, C6	100pF	100pF	100pF	Capacitor 0402
C8	100nF	100nF	100nF	Capacitor 0402
L1	**27nH**	**4.7nH**	**1.5nH**	Inductor 0402
R1	1 kohm	1 kohm	1 kohm	Resistor 0608
R2	30 kohm	30 kohm	30 kohm	Resistor 0608
C9, C10	1 kohm	1 kohm	1 kohm	Resistor 0402
C11	100nF	100nF	100nF	Capacitor 0402
C4, C7	N.C	N.C	N.C	

Figure 10. Recommended Application Circuits in Serial Mode

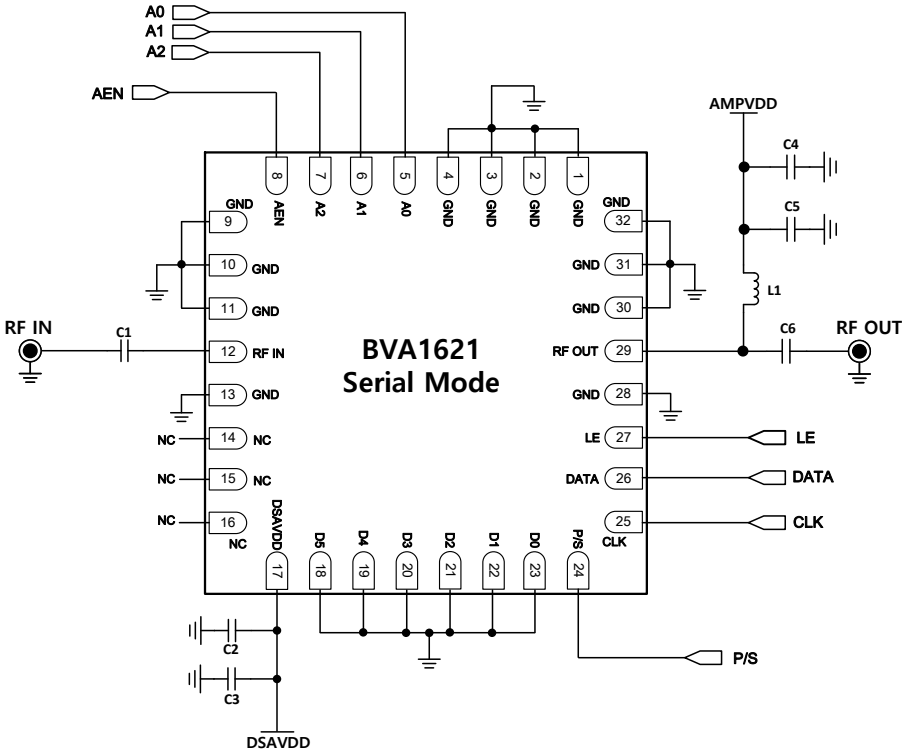


Figure 11. Recommended Application Circuits in Parallel Mode

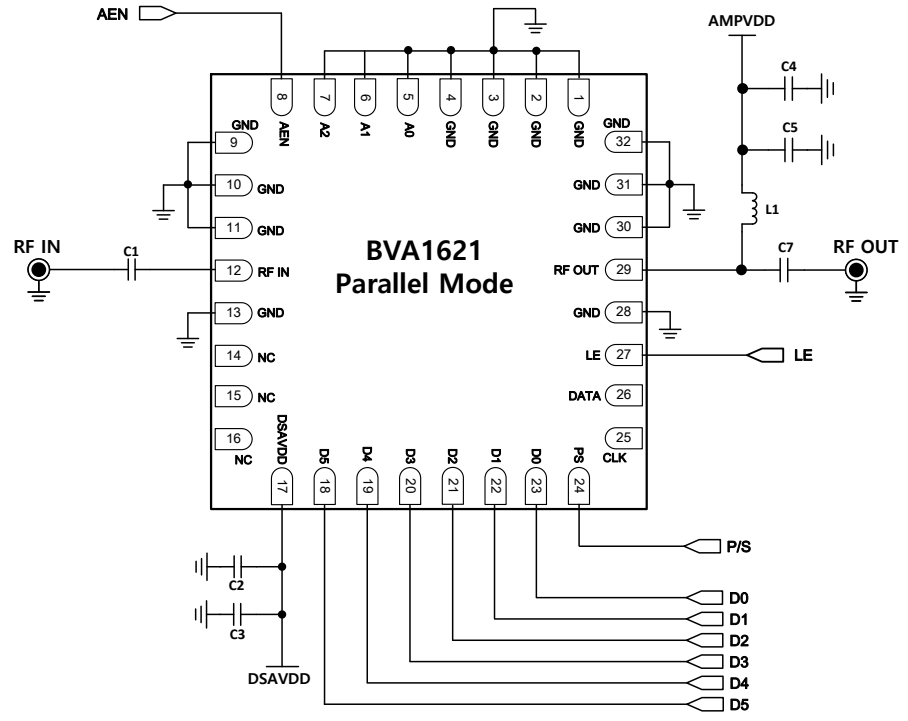
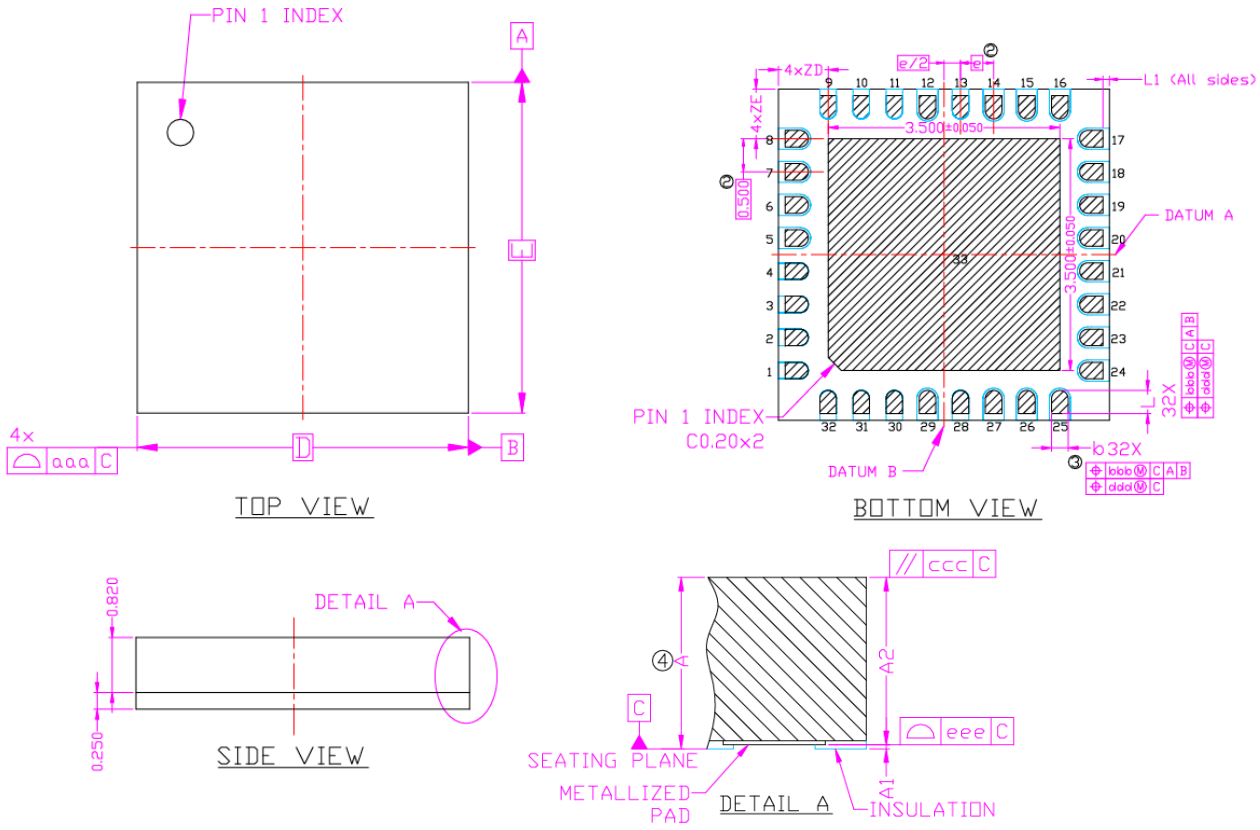


Figure 12. Package Outline Dimension



DIMENSIONAL REFERENCES unit: mm

REF.	Min.	Nom.	Max.
A	1.02	1.07	1.12
A1	-	-	0.03
A2	-	-	1.09
b	0.20	0.25	0.30
L	0.30	0.35	0.40
D	4.90	5.00	5.10
E	4.90	5.00	5.10
ZD	0.75 BSC		
ZE	0.75 BSC		
e	0.50 BSC		
L1	0.10 REF		

DIMENSIONAL REFERENCES unit: mm

REF.	TOLERANCE OF FORM AND POSITION
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.08
eee	0.08

Notes :
① ALL DIMENSION ARE IN MILLIMETER.
② 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
③ DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
④ DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
⑤ EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.
⑥ PACKAGE DIMENSIONS TAKE REFERENCE TO JEDEC MO-208 REV.C.

Figure 13. Package Marking

Marking information:	
BVA1621	Device Name
YY	Year
WW	Work Week
XX	Wafer Run Number

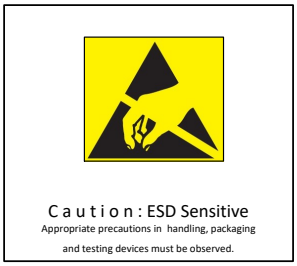
Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	TBD
Value:	TBD
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JS-001-2017
MSL Rating:	**Level 3 at +260°C convection reflow**
Standard:	JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

2	**N**	**9**	**6**	**F**