# BVA1621

## High Linearity wideband DVGA with addressable function

**400MHz - 4000MHz**

### Device Features

- Integrate DSA to AMP Functionality
- 400 - 4000MHz Broadband Performance
- Wide Supply Voltage Range
  AMP : 3.3V to 5.25V
  DSA : 2.7V to 5.5V
- Low current : 85mA @ 5V, 48mA @ 3.3V
- High Gain
  20.3dB@800MHz, 17.5dB@2.7GHz (VDD=5V)
  19.8dB@800MHz, 16.9dB@2.7GHz (VDD=3.3V)
- High OP1dB
  22dBm@800MHz, 21.6Bm@2.7GHz (VDD=5V)
  18.3dBm@800MHz, 18.1dBm@2.7GHz (VDD=3.3V)
- High OIP3
  36.5dBm@800MHz, 36.4dBm@2.7GHz (VDD=5V)
  32dBm@800MHz, 32.8dBm@2.7GHz (VDD=3.3V)
- Noise Figure at max gain setting
  1.7dB@800MHz, 2.6dB@2.7GHz (VDD=5V)
- Attenuation Range : Up to 31.5dB / 0.5dB step
- Safe attenuation state transitions
- Excellent attenuation accuracy
  ±(0.15 + 3% x ATT) @800MHz
  ±(0.25 + 3% x ATT) @2.7GHz
- Programming modes
  Serial mode with Addressable function
  Latched Parallel Mode
  Direct Parallel Mode
- 3bit Addressable function
  LE/SERIN/CLK can be shared up to 8EA Chips
- Lead-free/RoHS2-compliant 32-lead 5mm x 5mm x 1.07mm SIP LGA SMT package


32-lead 5mm x 5mm x 1.07mm SIP LGA

**Figure 1. Package Type**

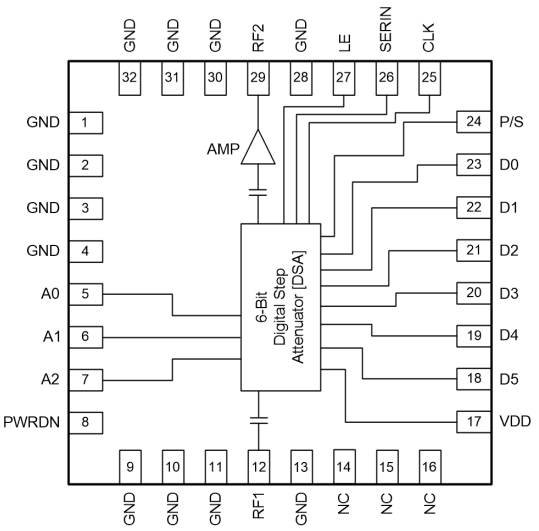



**Figure 2. Functional Block Diagram**

### Product Description

The BVA1621 is a high performance, digitally controlled variable gain amplifier (DVGA) operating from 400MHz to 4GHz.

The BVA1621 integrates a high performance digital step attenuator (DSA) and a high linearity, broadband gain block amplifier operating voltage 3.3V to 5.25V DC within enable control using the small package.

Both DSA and gain block amplifier in BVA1621 are internally matched to 50 ohms and It is easy to use with minimum external matching components required.

The BVA1621 can control 6-bit attenuation to 0.5dB step up to 31.5dB and initialize to the maximum attenuation setting on power-up until next programming word is inputted.
In addition, Internal DSA has a 3-bit addressable function, so it can share up to 8 DSAs(or DVGAs) Latch Enable(LE), SERIN and CLOCK (CLK) pin. This has the advantage of reducing the number of IO pins when using multiple DSA or DVGA chip with addressable function.

The BVA1621 is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless application.

### Application

- 5G/4G/3G Wireless infrastructure and other high performance RF application
- Microwave and Satellite Radio
- General purpose Wireless

### Table 1. Electrical Specifications[1] @ VDD = 5V

| Parameter | | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operational Frequency Range | | | 400 | | 4000 | MHz |
| Gain[2] | | ATT = 0dB @ 800MHz | | 20.3 | | dB |
| | | ATT = 0dB @ 1.8GHz | | 18.6 | | |
| | | ATT = 0dB @ 2.7GHz | | 17.5 | | |
| | | ATT = 0dB @ 3.5GHz | | 16.8 | | |
| Attenuation Control range | | 0.5dB Step | | 0 - 31.5 | | dB |
| Attenuation Step | | | | 0.5 | | dB |
| Attenuation Accuracy | 400MHz - 1GHz | Any bit or bit combination | | | ±(0.15 + 3% of ATT setting) | dB |
| | 1GHz - 2GHz | | | | ±(0.25 + 3% of ATT setting) | |
| | 2GHz - 3GHz | | | | ±(0.25 + 3% of ATT setting) | |
| | 3GHz - 4GHz | | | | ±(0.25 + 5% of ATT setting) | |
| Input Return loss | 400MHz - 2GHz | ATT = 0dB | | -10 | | dB |
| | 2GHz - 4GHz | | | -11 | | |
| Output Return loss | 400MHz - 2GHz | ATT = 0dB | | -11 | | dB |
| | 2GHz - 4GHz | | | -10 | | |
| Output Power for 1dB Compression | | ATT = 0dB @ 800MHz | | 22.0 | | dBm |
| | | ATT = 0dB @ 1.8GHz | | 21.9 | | |
| | | ATT = 0dB @ 2.7GHz | | 21.6 | | |
| | | ATT = 0dB @ 3.5GHz | | 21.1 | | |
| Output Third Order Intercept Point[3] | | ATT = 0dB @ 800MHz | | 36.5 | | dBm |
| | | ATT = 0dB @ 1.8GHz | | 36.3 | | |
| | | ATT = 0dB @ 2.7GHz | | 36.4 | | |
| | | ATT = 0dB @ 3.5GHz | | 37.0 | | |
| Noise Figure | | ATT = 0dB @ 800MHz | | 1.7 | | dB |
| | | ATT = 0dB @ 1.8GHz | | 2.2 | | |
| | | ATT = 0dB @ 2.7GHz | | 2.6 | | |
| | | ATT = 0dB @ 3.5GHz | | 2.9 | | |
| DSA Switching time | | 50% CTRL(LE) to 90% or 10% RF | | 500 | 800 | ns |
| AMP Switching time | | 50% CTRL(PWRDN) to 90% or 10% RF | | 150 | | ns |
| Impedance | | | | 50 | | Ω |

1. Device performance : measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+5.0V.
2. Gain data has PCB & Connectors insertion loss de-embedded.
3. OIP3 measured with two tones at an output of 3dBm per tone separated by 1MHz.

### Table 2. Electrical Specifications[1] @ VDD = 3.3V

| Parameter | | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operational Frequency Range | | | 400 | | 4000 | MHz |
| Gain[2] | | ATT = 0dB @ 800MHz | | 19.8 | | dB |
| | | ATT = 0dB @ 1.8GHz | | 18.1 | | |
| | | ATT = 0dB @ 2.7GHz | | 16.9 | | |
| | | ATT = 0dB @ 3.5GHz | | 16.3 | | |
| Attenuation Control range | | 0.5dB Step | | 0 - 31.5 | | dB |
| Attenuation Step | | | | 0.5 | | dB |
| Attenuation Accuracy | 400MHz - 1GHz | Any bit or bit combination | | | ±(0.15 + 3% of ATT setting) | dB |
| | 1GHz - 2GHz | | | | ±(0.25 + 3% of ATT setting) | |
| | 2GHz - 3GHz | | | | ±(0.25 + 3% of ATT setting) | |
| | 3GHz - 4GHz | | | | ±(0.25 + 5% of ATT setting) | |
| Input Return loss | 400MHz - 2GHz | ATT = 0dB | | -10 | | dB |
| | 2GHz - 4GHz | | | -10 | | |
| Output Return loss | 400MHz - 2GHz | ATT = 0dB | | -10 | | dB |
| | 2GHz - 4GHz | | | -10 | | |
| Output Power for 1dB Compression | | ATT = 0dB @ 800MHz | | 18.3 | | dBm |
| | | ATT = 0dB @ 1.8GHz | | 18.5 | | |
| | | ATT = 0dB @ 2.7GHz | | 18.1 | | |
| | | ATT = 0dB @ 3.5GHz | | 17.8 | | |
| Output Third Order Intercept Point[3] | | ATT = 0dB @ 800MHz | | 32.0 | | dBm |
| | | ATT = 0dB @ 1.8GHz | | 32.5 | | |
| | | ATT = 0dB @ 2.7GHz | | 32.8 | | |
| | | ATT = 0dB @ 3.5GHz | | 33.8 | | |
| Noise Figure | | ATT = 0dB @ 800MHz | | 1.6 | | dB |
| | | ATT = 0dB @ 1.8GHz | | 2.2 | | |
| | | ATT = 0dB @ 2.7GHz | | 2.6 | | |
| | | ATT = 0dB @ 3.5GHz | | 2.9 | | |
| DSA Switching time | | 50% CTRL(LE) to 90% or 10% RF | | 500 | 800 | ns |
| AMP Switching time | | 50% CTRL(PWRDN) to 90% or 10% RF | | 150 | | ns |
| Impedance | | | | 50 | | Ω |

1. Device performance : measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+3.3V.
2. Gain data has PCB & Connectors insertion loss de-embedded.
3. OIP3 measured with two tones at an output of 3dBm per tone separated by 1MHz.

**Table 3. Absolute Maximum Ratings**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Supply Voltage** | AMP | | | 5.5 | V |
| | DSA | | | 5.5 | V |
| **Supply Current** | AMP | | | 190 | mA |
| | DSA | | | 1000 | uA |
| **Digital input voltage** | AMP Control Pin (PWRDN) | -0.3 | | 5.25 | V |
| | DSA Control Pin ( LE, SERIN, CLK, P/S, D0 - D5, A0, A1, A2 ) | -0.3 | | 3.6 | V |
| **Maximum input power** | AMP | | | 20 | dBm |
| | DSA | | | 30 | dBm |
| **Storage Temperature** | | -55 | | 150 | ℃ |
| **Junction Temperature** | | | 150 | | ℃ |

Operation of this device above any of these parameters may result in permanent damage.

**Table 4. Recommended Operating Conditions**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Frequency Range** | DSA + AMP | 400 | | 4000 | MHz |
| **Supply Voltage, VDD** | AMP VDD | 3.3 | 5 | 5.25 | V |
| | DSA VDD | 2.7 | | 5.5 | V |
| **Current, IDD** | AMP ON @ VDD=5V | | 85 | | mA |
| | AMP ON @ VDD=3.3V | | 48 | | mA |
| | AMP OFF | | | 7 | mA |
| | DSA | | 200 | | uA |
| **PWRDN Control Voltage** | AMP ON | 0 | | 0.6 | V |
| | AMP OFF | 1.17 | | VDD | V |
| **PWRDN pin Current** | AMP OFF | | 150 | | uA |
| **DSA Control Voltage** | Digital Input High | 1.17 | | 3.6 | V |
| | Digital Input Low | -0.3 | | 0.6 | V |
| **DSA Control pin Current** | Digital Input High | | | 20 | uA |
| **Operating Temperature** | DSA + AMP | -40 | | 125 | ℃ |

Specifications are not guaranteed over all recommended operating conditions.

**Table 5. Package Thermal Characteristics**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| **Junction to Ambient Thermal Resistance** | $\theta_{JA}$ | TBD | °C/W |

**Figure 3. Pin Configuration (Top View)**

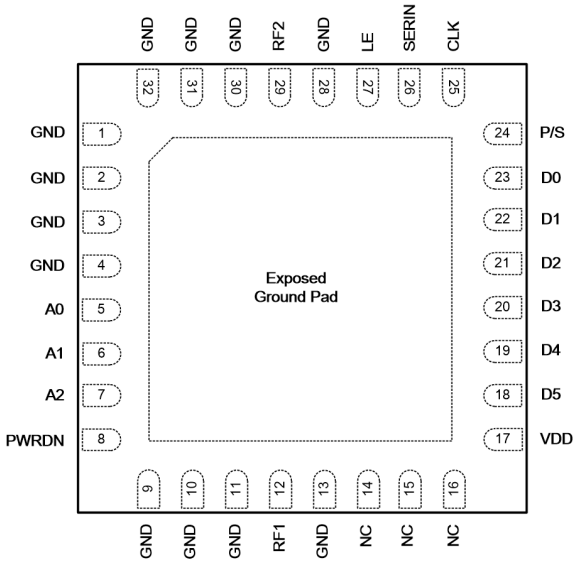



**Table 6. Pin Description**

| Pin | Pin name | Description |
|---|---|---|
| **5** | A0 | Address bit A0 connection |
| **6** | A1 | Address bit A1 connection |
| **7** | A2 | Address bit A2 connection |
| **8** | PWRDN | Amplifier Power Down ( 0 = Amp ON, 1 = AMP Power Down ) |
| **12** | RF1 | RF Input ( DSA RF Input ) |
| **17** | VDD | DSA Supply Voltage ( 2.7V to 5.5V ) |
| **18** | D5[1] | DSA Attenuation 16dB Control Word : MSB |
| **19** | D4[1] | DSA Attenuation 8dB Control Word |
| **20** | D3[1] | DSA Attenuation 4dB Control Word |
| **21** | D2[1] | DSA Attenuation 2dB Control Word |
| **22** | D1[1] | DSA Attenuation 1dB Control Word |
| **23** | D0[1] | DSA Attenuation 0.5dB Control Word : LSB |
| **24** | P/S | DSA Control Mode Selection ( 1 = Serial Mode, 0 = Parallel Mode ) |
| **25** | CLK | SPI Clock Input |
| **26** | SERIN | SPI Data Input |
| **27** | LE | Latch Enable |
| **29** | RF2 | RF Output ( AMP RF Output and Supply Voltage : 3.3V to 5.25V ) |
| **14, 15, 16** | NC | Not Connected |
| **Others** | GND | Ground, These pins must be connected to ground |

1. It is recommended to ground the D0 ~ D5 in serial mode.

## Programming Options

BVA1621 can be programmed using either the parallel or serial interface, which is selectable via P/S pin(Pin24).
Serial mode is selected by pulling it to a voltage logic HIGH and parallel mode is selected by setting P/S to logic LOW.

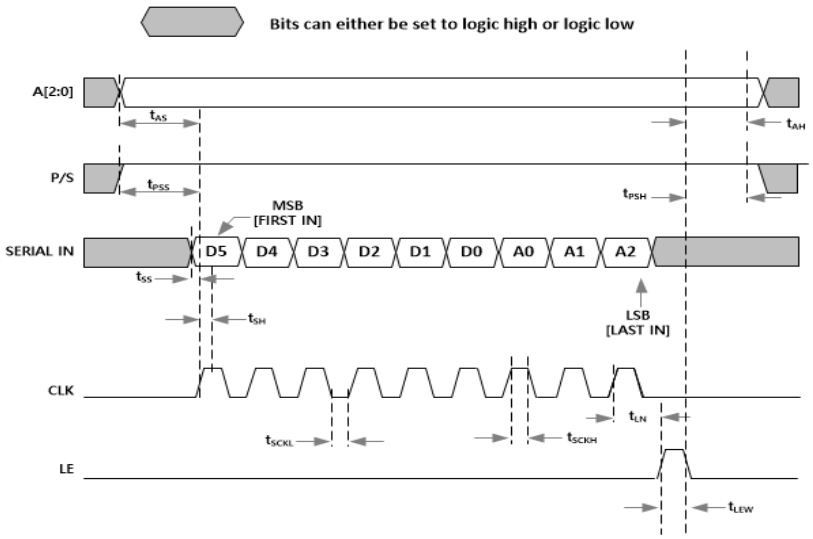
### *Serial Control Mode*

The serial interface is a 6-bit shift register to shift in the data MSB (D5) first. When serial programming is used, It is recommended all the parallel control input pins ( 18, 19, 20, 21, 22, 23 ) are grounded .
It is controlled by three CMOS-compatible signals: SERIN, Clock, and Latch Enable (LE).

**Table 7. Truth Table for Serial Control Word**

| Digital Control Input | | | | | | Attenuation State [dB] |
|---|---|---|---|---|---|---|
| D5 (MSB) | D4 | D3 | D2 | D1 | D0 (LSB) | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0.5 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 2 |
| 0 | 0 | 1 | 0 | 0 | 0 | 4 |
| 0 | 1 | 0 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 0 | 0 | 0 | 16 |
| 1 | 1 | 1 | 1 | 1 | 1 | 31.5 |

**Figure 4. Serial Mode Timing Diagram**




BVA1621 Serial mode is selected by pulling it to logic HIGH. The serial interface is a 9-bit shift register made up of two words. The first 6-bit word is the Attenuation word, which controls the DSA state. The second word is the address word, which uses 3 bits that must match the hard wired A0-A2 programming in order to change the DSA state. If no external connections are made to A0-A2 then internally they will default to 000 due to internal pull down resistors. If these 3 external preset address bits are not matched with the SPI loaded address bits, then the current attenuator state will remain unchanged. This allows up to 8 serial-controlled devices to be used on a single board, which share a common SERIN, CLK and LE.

When serial programming is used, all the parallel control input pins 18, 19, 20, 21, 22, 23 can be left grounded or open.

**Table 8. Serial Interface Timing Specifications**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{CLK}$ | Serial data clock frequency | | | 10 | MHz |
| $t_{AS}$ | Address setup time | 100 | | | ns |
| $t_{AH}$ | Address hold time | 100 | | | ns |
| $t_{PSS}$ | Parallel/Serial setup time | 100 | | | ns |
| $t_{PSH}$ | Parallel/Serial hold time | 100 | | | ns |
| $t_{SCK}$ | Minimum serial period | 70 | | | ns |
| $t_{SS}$ | Serial Data setup time | 10 | | | ns |
| $t_{SH}$ | Serial Data hold time | 10 | | | ns |
| $t_{LN}$ | LE setup time | 10 | | | ns |
| $t_{LEW}$ | Minimum LE pulse width | 30 | | | ns |

**Figure 5. Multi Device Addressing Scheme using SPI**

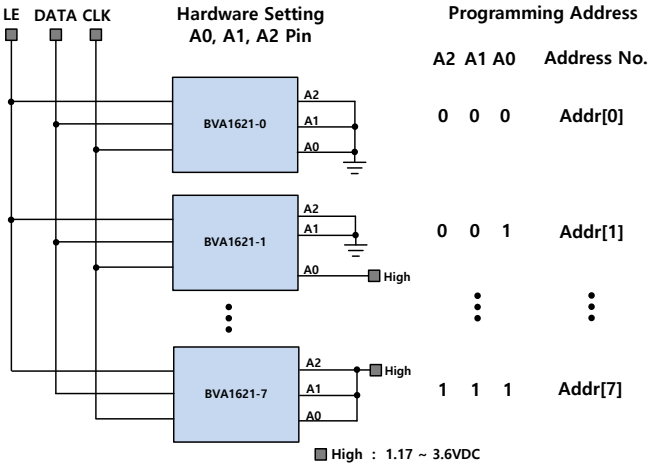



**Table 9. Truth Table for Address Control Word**

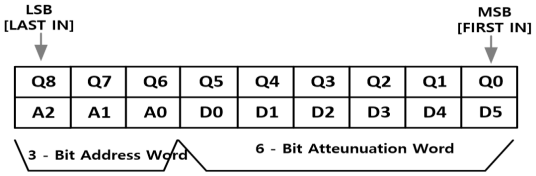
| Address Digital Control Input | | | Address Setting | Address No. |
|---|---|---|---|---|
| A2 | A1 | A0 | | |
| 0 | 0 | 0 | 000 | Addr[0] |
| 0 | 0 | 1 | 001 | Addr[1] |
| 0 | 1 | 0 | 010 | Addr[2] |
| 0 | 1 | 1 | 011 | Addr[3] |
| 1 | 0 | 0 | 100 | Addr[4] |
| 1 | 0 | 1 | 101 | Addr[5] |
| 1 | 1 | 0 | 110 | Addr[6] |
| 1 | 1 | 1 | 111 | Addr[7] |

### *Serial Register Map*

The BVA1621 can be programmed via the serial control on the rising edge of Latch Enable (LE) which loads the last 6-bits attenuation word and 3-bits address word in the SHIFT Register. Data is clocked in MSB(D5) first.

The shift register must be loaded while LE is kept LOW to prevent changing the attenuation value during data is inputted.

**Figure 6. Serial Register Map**




The serial register consist of 9-bits as shown in Figure 6. First 6-bits from LSB are Attenuation word, 3-bits after that are Address word. The Attenuation word is DSA attenuation control bit and the Address word is static logical bit determined by A0, A1 and A2 digital inputs. The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by two because of 0.5dB step up to 31.5dB ( total 63 Attenuation state), then convert to binary.

For example, to program attenuation 15.5dB state of Addr[5] BVA1621 :

Attenuation State
2 x 15.5 = 31
D0 - D5 : 111110

Address state
Digital input of A2, A1, A0 pin = 101

Serial DATA Input : 101111110

| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| A2 | A1 | A0 | D0 | D1 | D2 | D3 | D4 | D5 |

### *Power-UP states Settings*

The BVA1621 will always initialize to the maximum attenuation setting (31.5 dB) on power-up for both the Serial and Latched Parallel modes of operation and will remain in this setting until the user latches in the next programming word. In Direct Parallel mode, the DSA can be preset to any state within the 31.5 dB range by pre-setting the Parallel control pins prior to power-up.

## Programming Options

### *Parallel Control Mode*

The parallel control interface has six digital control input lines (D5 to D0) to set the attenuation value. D5 is the most significant bit (MSB) that selects the 16 dB attenuator stage, and D0 is the least significant bit (LSB) that selects the 0.5 dB attenuator stage.

### *Direct Parallel Mode*

For direct parallel mode, The LE pin must be kept HIGH. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator. In this mode the device will immediately react to any voltage changes to the parallel control pins [ pins 18, 19, 20, 21, 22, 23 ]. Use direct parallel mode for the fastest settling time.

### *Latched Parallel Mode*

The LE pin must be kept LOW when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled HIGH to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled LOW to latch the change into the device until the next desired attenuation change (see Figure 7 and Table 10).

- Set P/S is logic LOW.
- Set LE to logic LOW.
- Adjust pins [ 18, 19, 20, 21, 22, 23 ] to the desired attenuation setting. (Note the device will not react to these pins while LE is a logic LOW).
- Pull LE to a logic HIGH. The device will then transition to the attenuation settings reflected by pins D5 - D0.
- If LE is pulled to a logic LOW then the attenuator will not change state.

Latched Parallel Mode implies a default state for when the device is first powered up with P/S pin set for logic LOW and LE logic LOW. In this case the default setting is **Maximum attenuation** .

**Table 10. Truth Table for the Parallel Control Word**

| D5 | D4 | D3 | D2 | D1 | D0 | P/S | LE | Attenuation State(dB) |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 (RL) |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0.5 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1.0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 2.0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 4.0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 8.0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 16.0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 31.5 |

**Figure 7. Latched Parallel Mode Timing Diagram**

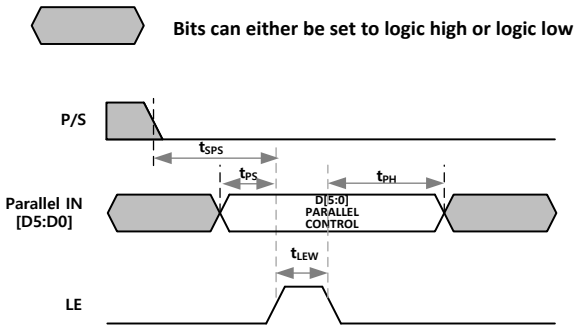



**Table 11. Parallel Interface Timing Specifications**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SPS}$ | Serial to Parallel Mode Setup Time | 100 | | | ns |
| $t_{LEW}$ | Minimum LE pulse width | 10 | | | ns |
| $t_{PH}$ | Data hold time from LE | 10 | | | ns |
| $t_{PS}$ | Data setup time to LE | 10 | | | ns |

## Switching Feature Description

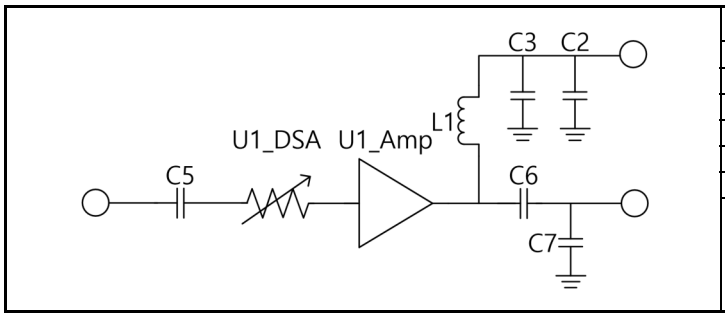
### *Glitch-Safe Attenuation State Transient*

The BVA1621 is the latest product applied *Glitch-Safe* technology with less than 1dB ringing (positive/negative) across the attenuation range when changing attenuation states. This technology protects Amplifiers or ADC during transitions between attenuation states.

## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 0.4 ~ 1.2GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 12**

**Table 12. 0.4 ~ 1.2GHz RF Application Circuit**




| BOM | |
|---|---|
| L1 | 33nH |
| C2 | 100nF |
| C3 | 100pF |
| C5 | 100pF |
| C6 | 100pF |
| C7 | 0.8pF |

This value can be changed little by little according to the frequency band and bandwidth.

**Table 13. Typical RF Performance @ VDD = 5V**

| Parameter | Frequency | | | Unit |
|---|---|---|---|---|
| | 500 | 800 | 1000 | MHz |
| **Gain**[1] | 20.5 | 20.3 | 19.9 | dB |
| **S11** | -10.7 | -11.2 | -10.0 | dB |
| **S22** | -14.5 | -14.1 | -11.3 | dB |
| **OIP3**[2] | 37.6 | 36.5 | 35.5 | dBm |
| **P1dB** | 22.0 | 22.0 | 21.8 | dBm |
| **Noise Figure** | 1.8 | 1.7 | 1.8 | dB |

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 measured with two tones at an output of 3 dBm per tone separated by 1 MHz.

**Table 14. Typical RF Performance @ VDD = 3.3V**

| Parameter | Frequency | | | Unit |
|---|---|---|---|---|
| | 500 | 800 | 1000 | MHz |
| **Gain**[1] | 20.0 | 19.8 | 19.3 | dB |
| **S11** | -10.0 | -10.2 | -9.2 | dB |
| **S22** | -14.0 | -12.9 | -10.4 | dB |
| **OIP3**[2] | 32.7 | 32.0 | 31.1 | dBm |
| **P1dB** | 18.3 | 18.3 | 18.0 | dBm |
| **Noise Figure** | 1.8 | 1.6 | 1.7 | dB |

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 measured with two tones at an output of 3 dBm per tone separated by 1 MHz.

**Figure 8. Gain vs. Frequency @ VDD = 5V**
Over Temperature

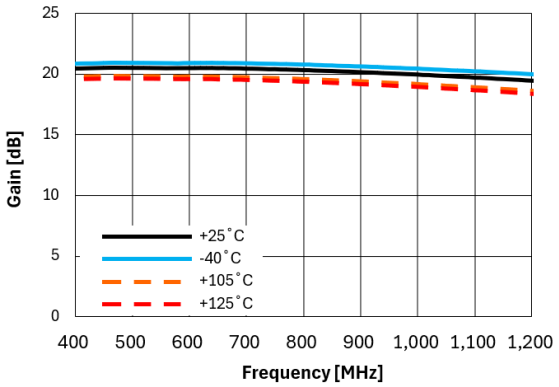
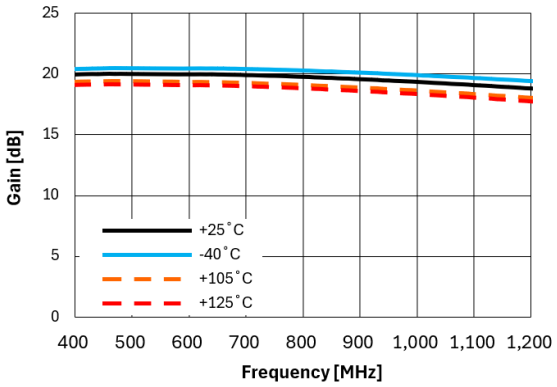



**Figure 9. Gain vs. Frequency @ VDD = 3.3V**
Over Temperature



## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 0.4 ~ 1.2GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 12**

**Figure 10. Gain vs. Frequency**
Over Major Attenuation States

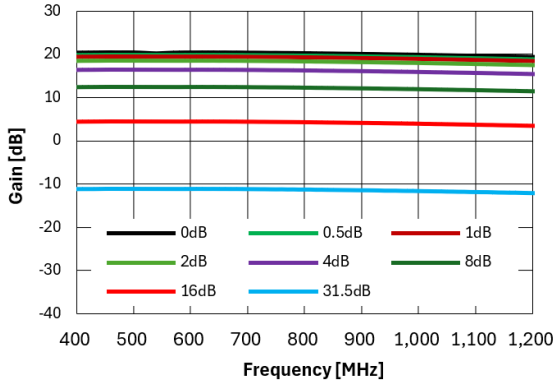



**Figure 11. Gain vs. Frequency vs VDD**
Max Gain States

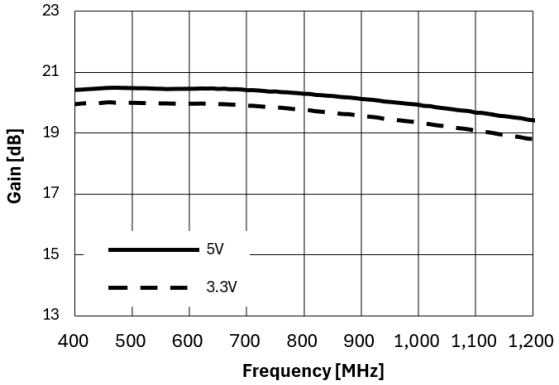



**Figure 12. Input Return Loss vs. Frequency**
Over Temperature (Min[1] / Max Gain State)

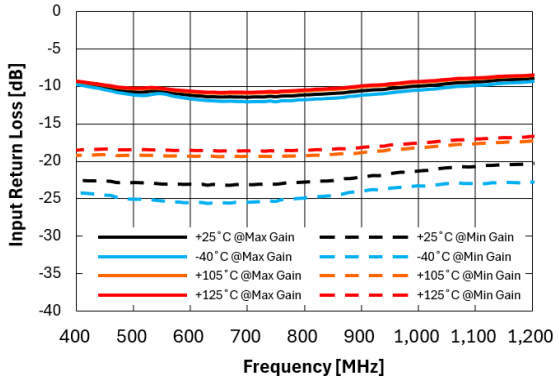
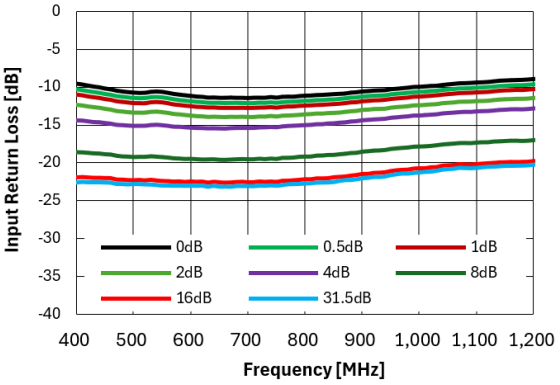



**Figure 13. Input Return Loss vs. Frequency**
Over Major Attenuation States




1.Min Gain was measured in the state is set with attenuation 31.5dB.

**Figure 14. Output Return Loss vs. Frequency**
Over Temperature (Min[1] / Max Gain State)

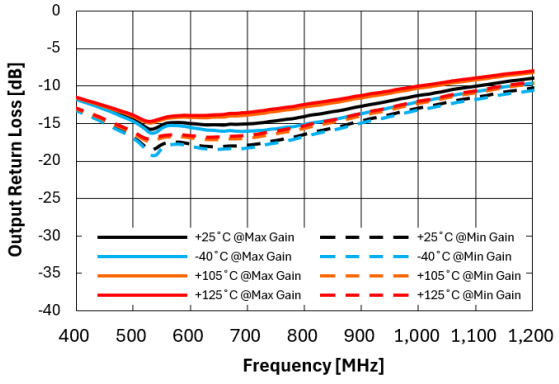
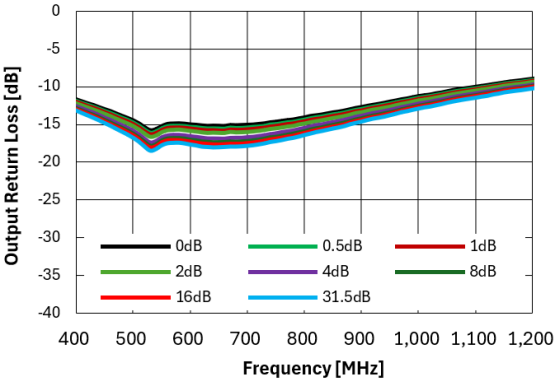



**Figure 15. Output Return Loss vs. Frequency**
Over Major Attenuation States




1.Min Gain was measured in the state is set with attenuation 31.5dB.

## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 0.4 ~ 1.2GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 12**

**Figure 16. K Factor vs Frequency**
Over Temperature (Max Gain State)

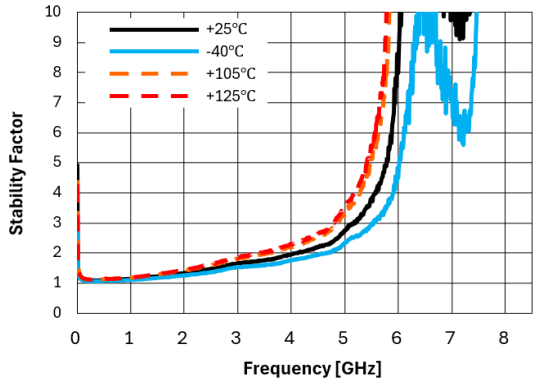



**Figure 17. OIP3 vs. Frequency vs. VDD**
Over Temperature (Max Gain State)

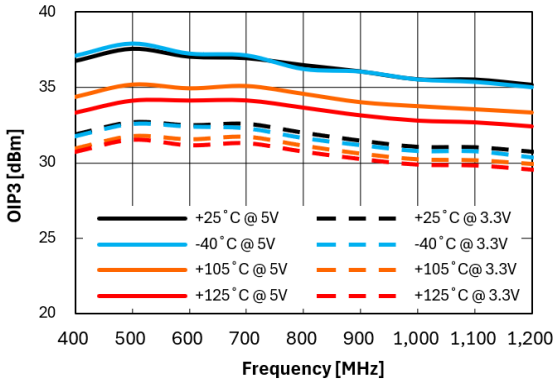



**Figure 18. OIP3 vs. Frequency vs. VDD**
Over Temperature (15.5dB Attenuation State)

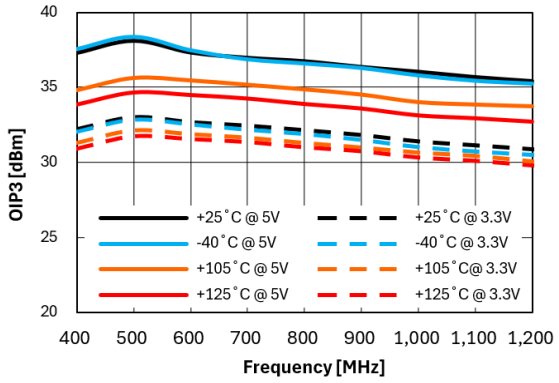



**Figure 19. P1dB vs. Frequency vs. VDD**
Over Temperature (Max Gain State)

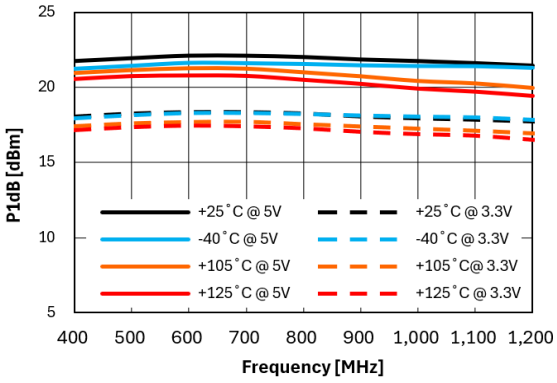



**Figure 20. Noise Figure vs. Frequency @ VDD = 5V**
Over Temperature (Max Gain State)

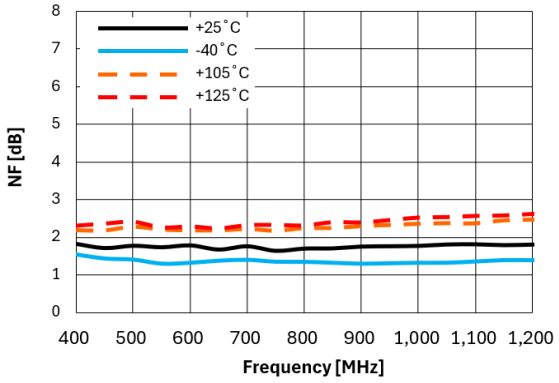
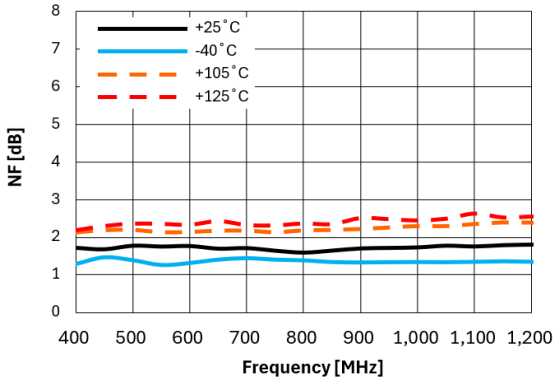



**Figure 21. Noise Figure vs. Frequency @ VDD = 3.3V**
Over Temperature (Max Gain State)



## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 0.4 ~ 1.2GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 12**

**Figure 22. Attenuation Error vs Frequency**
Over Major Attenuation Steps

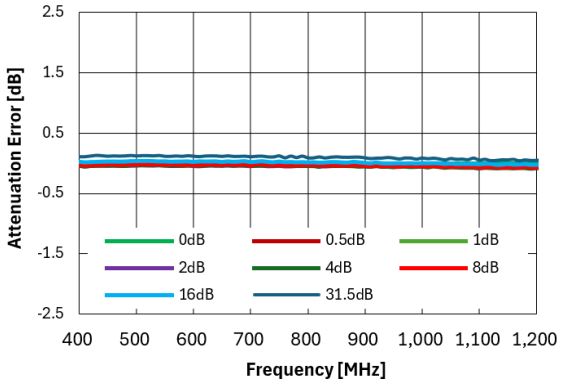



**Figure 23. Attenuation Error vs Attenuation Setting**
Over Major Frequency (Max Gain State)

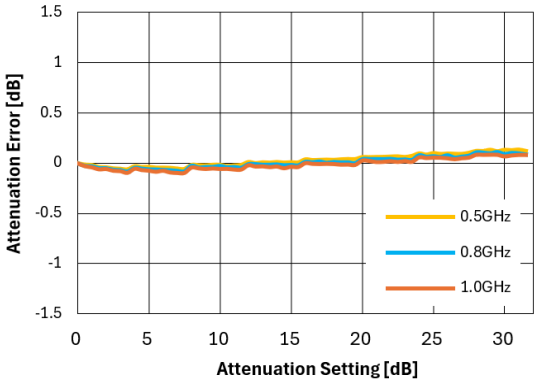



**Figure 24. Attenuation Error at 500MHz vs Temperature**
Over All Attenuation States

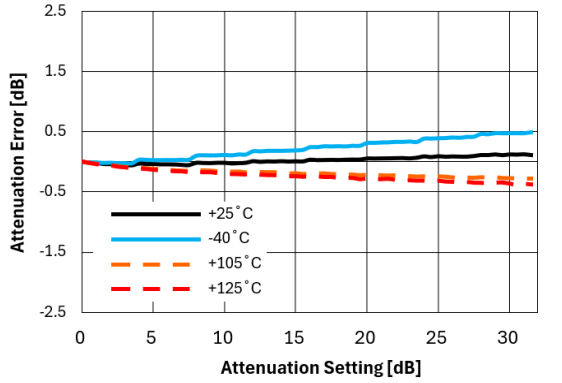



**Figure 25. Attenuation Error at 800MHz vs Temperature**
Over All Attenuation States

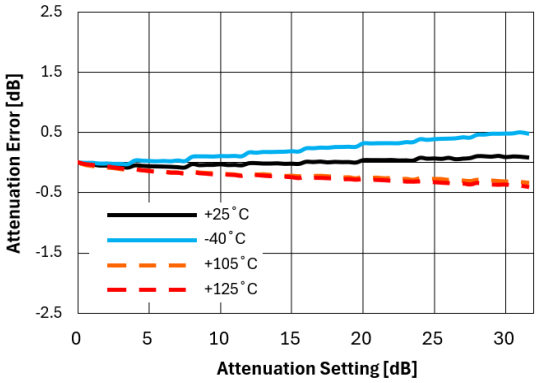
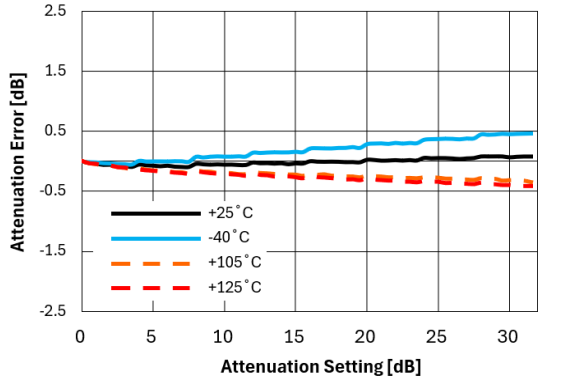


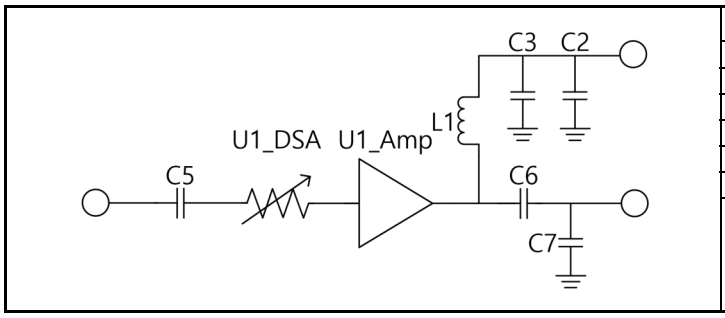

**Figure 26. Attenuation Error at 1.0GHz vs Temperature**
Over All Attenuation States



## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 1.5 ~ 2.3GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 15**

**Table 15. 1.5 ~ 2.3GHz RF Application Circuit**




| BOM | |
|---|---|
| L1 | 3.3nH |
| C2 | 100nF |
| C3 | 100pF |
| C5 | 100pF |
| C6 | 100pF |
| C7 | 0.7pF |

This value can be changed little by little according to the frequency band and bandwidth.

**Table 16. Typical RF Performance @ VDD = 5V**

| Parameter | Frequency | | | Unit |
|---|---|---|---|---|
| | 1700 | 1900 | 2100 | MHz |
| **Gain**[1] | 18.6 | 18.6 | 18.3 | dB |
| **S11** | -8.9 | -9.6 | -9.7 | dB |
| **S22** | -9.5 | -11.0 | -10.4 | dB |
| **OIP3**[2] | 36.4 | 36.2 | 36.2 | dBm |
| **P1dB** | 21.9 | 21.9 | 21.8 | dBm |
| **Noise Figure** | 2.2 | 2.3 | 2.3 | dB |

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 measured with two tones at an output of 3 dBm per tone separated by 1 MHz.

**Table 17. Typical RF Performance @ VDD = 3.3V**

| Parameter | Frequency | | | Unit |
|---|---|---|---|---|
| | 1700 | 1900 | 2100 | MHz |
| **Gain**[1] | 18.1 | 18.0 | 17.7 | dB |
| **S11** | -8.5 | -9.0 | -9.1 | dB |
| **S22** | -9.6 | -10.8 | -10.1 | dB |
| **OIP3**[2] | 32.6 | 32.4 | 32.2 | dBm |
| **P1dB** | 18.4 | 18.5 | 18.4 | dBm |
| **Noise Figure** | 2.1 | 2.2 | 2.3 | dB |

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 measured with two tones at an output of 3 dBm per tone separated by 1 MHz.

**Figure 27. Gain vs. Frequency @ VDD = 5V**
Over Temperature

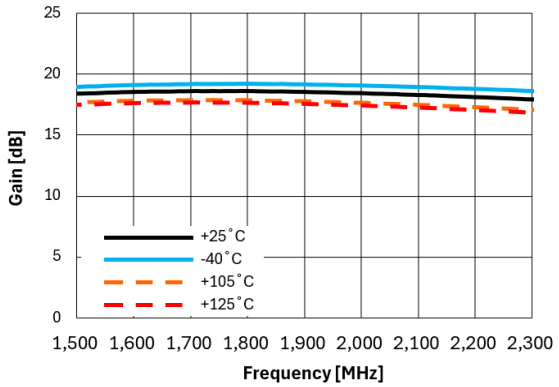
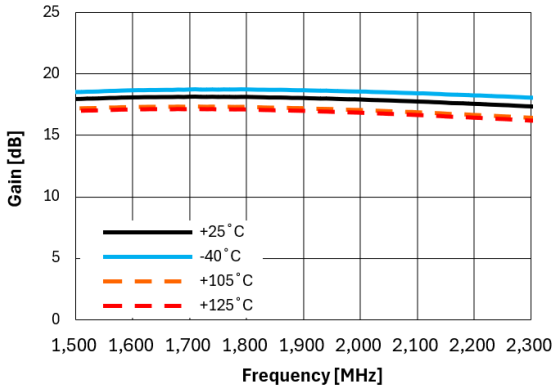



**Figure 28. Gain vs. Frequency @ VDD = 3.3V**
Over Temperature



## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 1.5 ~ 2.3GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 15**

**Figure 29. Gain vs. Frequency**
Over Major Attenuation States

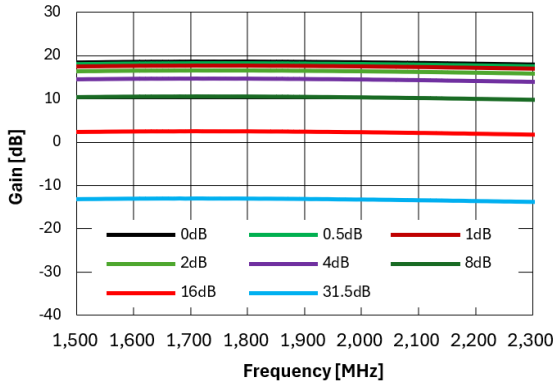



**Figure 30. Gain vs. Frequency vs VDD**
Max Gain States

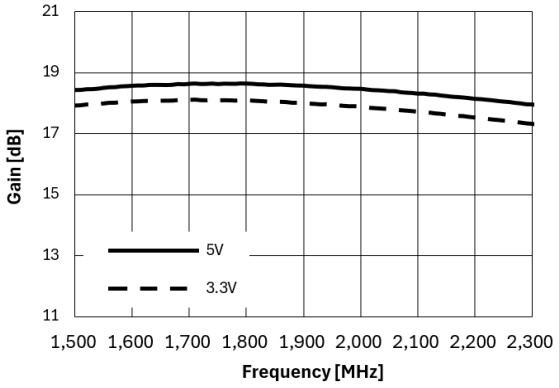



**Figure 31. Input Return Loss vs. Frequency**
Over Temperature (Min[1] / Max Gain State)

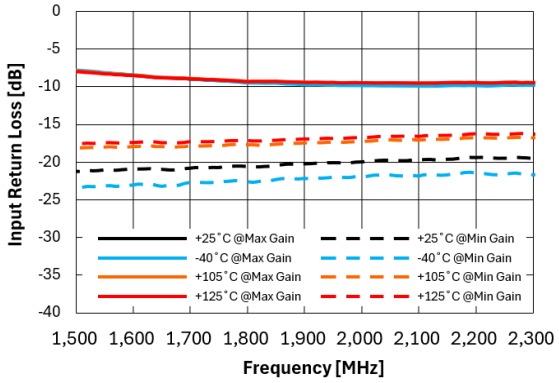
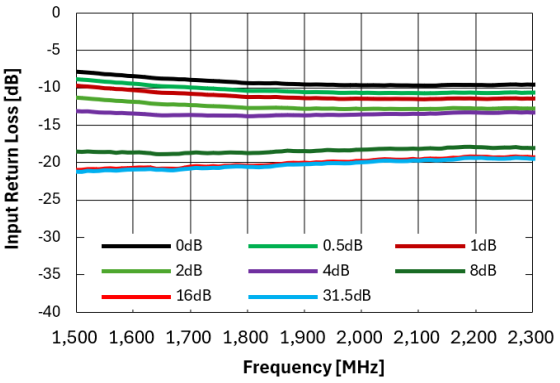



**Figure 32. Input Return Loss vs. Frequency**
Over Major Attenuation States




1.Min Gain was measured in the state is set with attenuation 31.5dB.

**Figure 33. Output Return Loss vs. Frequency**
Over Temperature (Min[1] / Max Gain State)

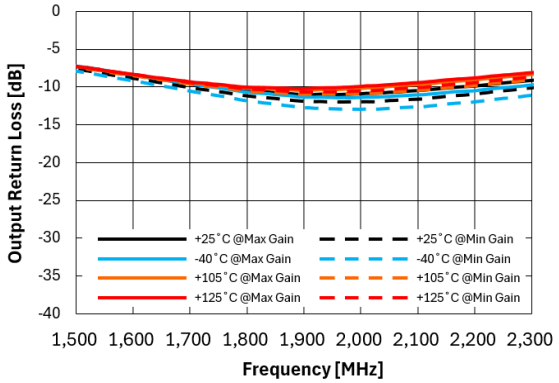
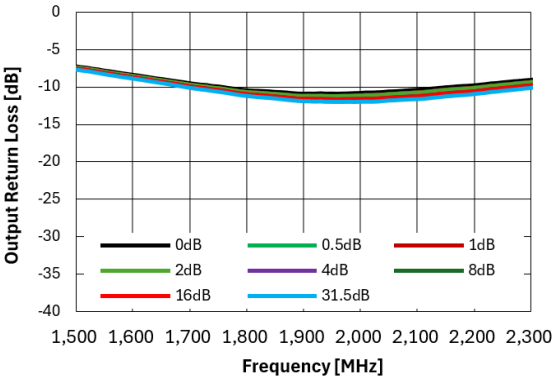



**Figure 34. Output Return Loss vs. Frequency**
Over Major Attenuation States




1.Min Gain was measured in the state is set with attenuation 31.5dB.

## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 1.5 ~ 2.3GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 15**

**Figure 35. K Factor vs Frequency**
Over Temperature (Max Gain State)

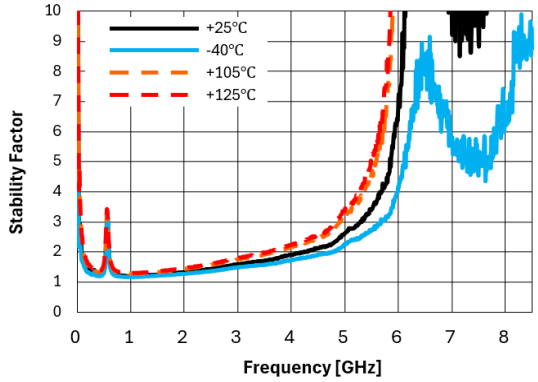



**Figure 36. OIP3 vs. Frequency vs. VDD**
Over Temperature (Max Gain State)

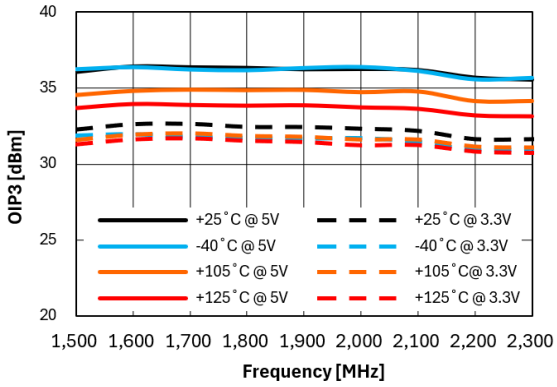



**Figure 37. OIP3 vs. Frequency vs. VDD**
Over Temperature (15.5dB Attenuation State)

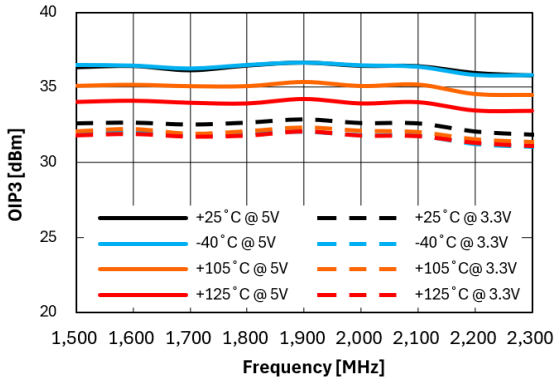



**Figure 38. P1dB vs. Frequency vs. VDD**
Over Temperature (Max Gain State)

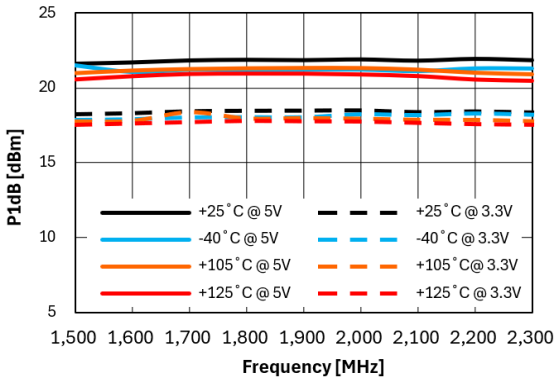



**Figure 39. Noise Figure vs. Frequency @ VDD = 5V**
Over Temperature (Max Gain State)

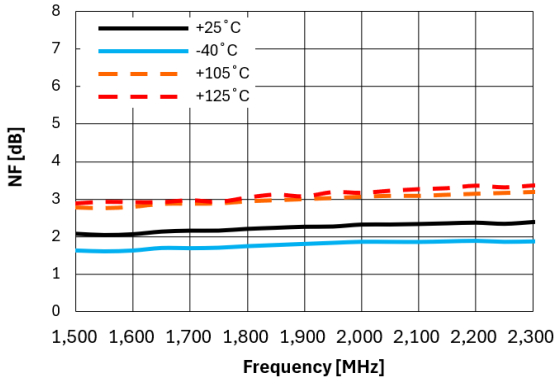
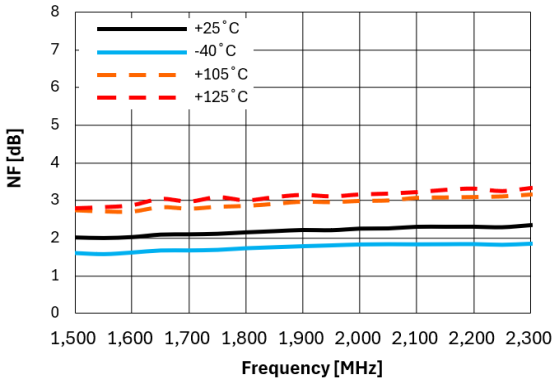



**Figure 40. Noise Figure vs. Frequency @ VDD = 3.3V**
Over Temperature (Max Gain State)



## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 1.5 ~ 2.3GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 15**

**Figure 41. Attenuation Error vs Frequency**
Over Major Attenuation Steps

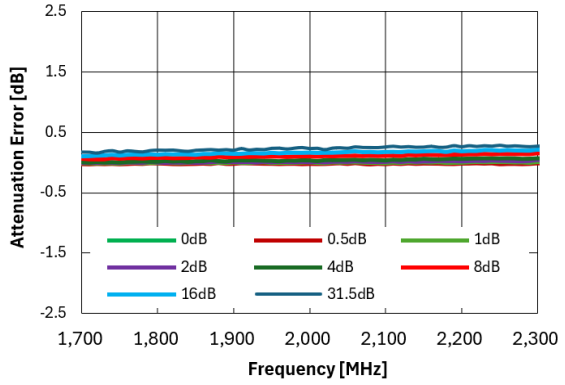



**Figure 42. Attenuation Error vs Attenuation Setting**
Over Major Frequency (Max Gain State)

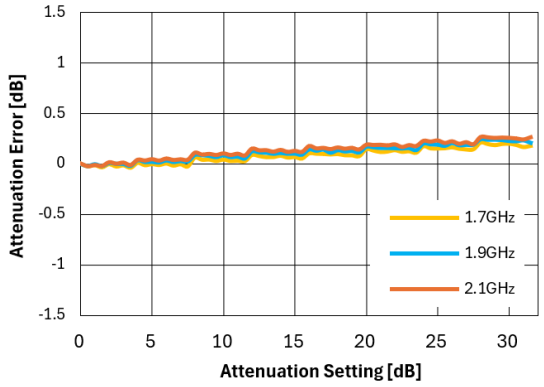



**Figure 43. Attenuation Error at 1.7GHz vs Temperature**
Over All Attenuation States

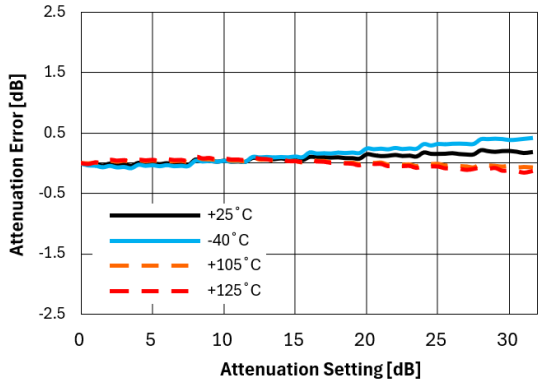



**Figure 44. Attenuation Error at 1.9GHz vs Temperature**
Over All Attenuation States

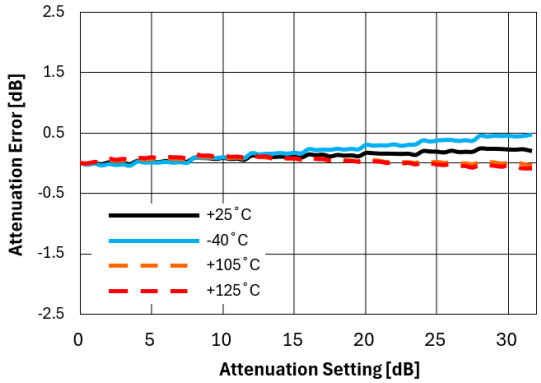
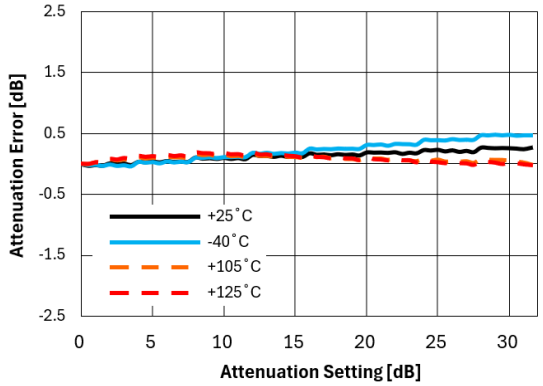


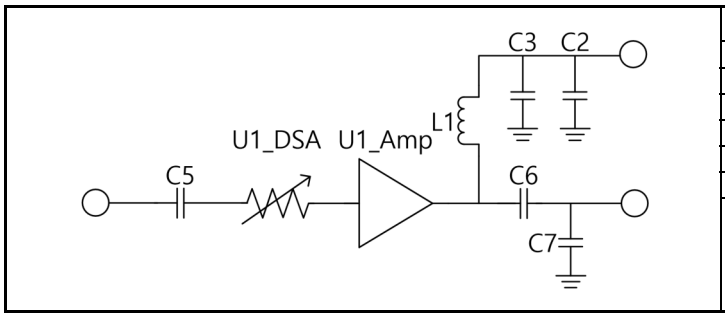

**Figure 45. Attenuation Error at 2.1GHz vs Temperature**
Over All Attenuation States



## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 2.3 ~ 3GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 18**

**Table 18. 2.3 ~ 3GHz RF Application Circuit**




| BOM | |
|---|---|
| L1 | 1.5nH |
| C2 | 100nF |
| C3 | 100pF |
| C5 | 100pF |
| C6 | 100pF |
| C7 | 0.7pF |

This value can be changed little by little according to the frequency band and bandwidth.

**Table 19. Typical RF Performance @ VDD = 5V**

| Parameter | Frequency | | | Unit |
|---|---|---|---|---|
| | 2300 | 2500 | 2700 | MHz |
| **Gain**[1] | 17.6 | 17.7 | 17.5 | dB |
| **S11** | -8.6 | -9.4 | -10.0 | dB |
| **S22** | -8.3 | -9.9 | -10.5 | dB |
| **OIP3**[2] | 36.0 | 36.5 | 36.4 | dBm |
| **P1dB** | 21.1 | 21.7 | 21.6 | dBm |
| **Noise Figure** | 2.5 | 2.5 | 2.6 | dB |

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 measured with two tones at an output of 3 dBm per tone separated by 1 MHz.

**Table 20. Typical RF Performance @ VDD = 3.3V**

| Parameter | Frequency | | | Unit |
|---|---|---|---|---|
| | 2300 | 2500 | 2700 | MHz |
| **Gain**[1] | 17.1 | 17.1 | 16.9 | dB |
| **S11** | -8.2 | -8.9 | -9.4 | dB |
| **S22** | -8.6 | -10.1 | -10.5 | dB |
| **OIP3**[2] | 32.5 | 32.8 | 32.8 | dBm |
| **P1dB** | 17.7 | 18.2 | 18.1 | dBm |
| **Noise Figure** | 2.4 | 2.5 | 2.6 | dB |

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 measured with two tones at an output of 3 dBm per tone separated by 1 MHz.

**Figure 46. Gain vs. Frequency @ VDD = 5V**
Over Temperature

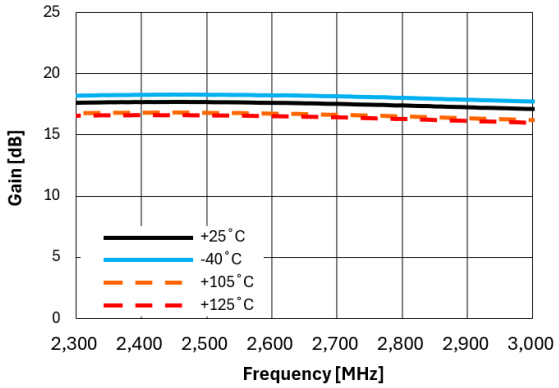
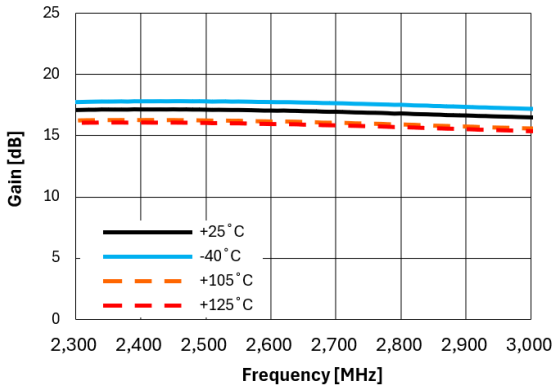



**Figure 47. Gain vs. Frequency @ VDD = 3.3V**
Over Temperature



## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 2.3 ~ 3GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 18**

**Figure 48. Gain vs. Frequency**
Over Major Attenuation States

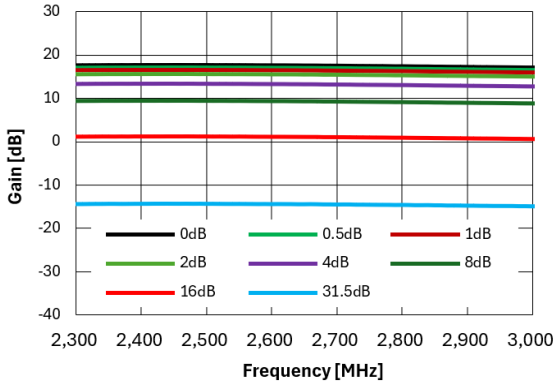



**Figure 49. Gain vs. Frequency vs VDD**
Max Gain States

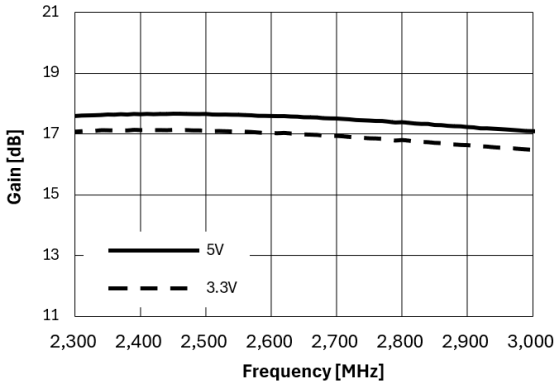



**Figure 50. Input Return Loss vs. Frequency**
Over Temperature (Min[1] / Max Gain State)

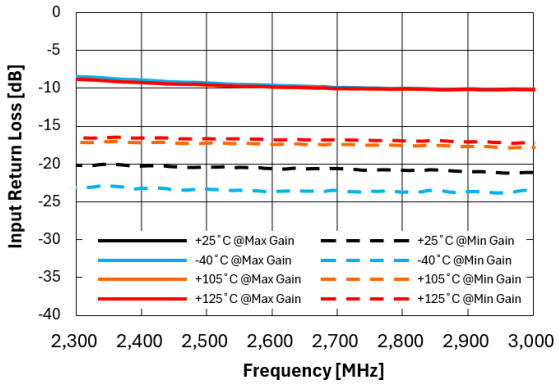
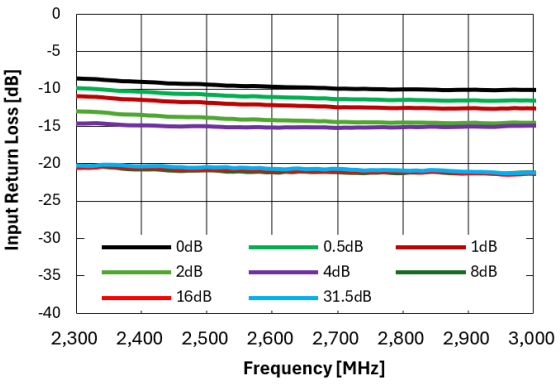



**Figure 51. Input Return Loss vs. Frequency**
Over Major Attenuation States




1.Min Gain was measured in the state is set with attenuation 31.5dB.

**Figure 52. Output Return Loss vs. Frequency**
Over Temperature (Min[1] / Max Gain State)

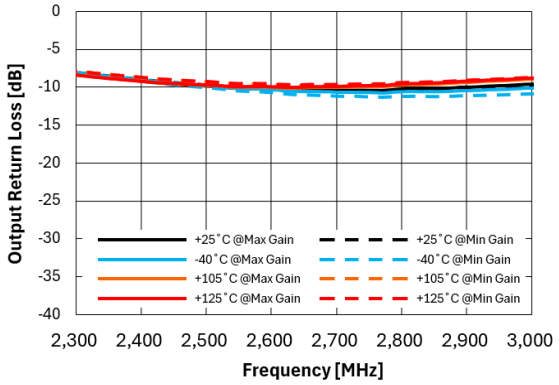
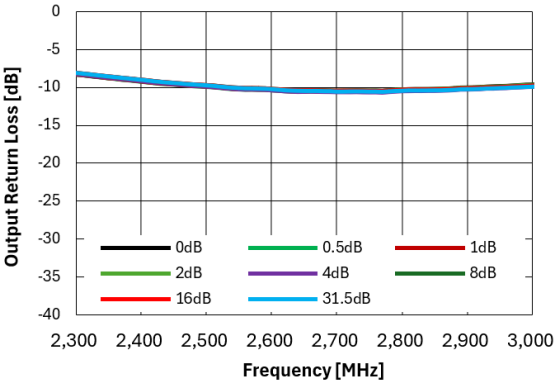



**Figure 53. Output Return Loss vs. Frequency**
Over Major Attenuation States




1.Min Gain was measured in the state is set with attenuation 31.5dB.

## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 2.3 ~ 3GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 18**

**Figure 54. K Factor vs Frequency**
Over Temperature (Max Gain State)

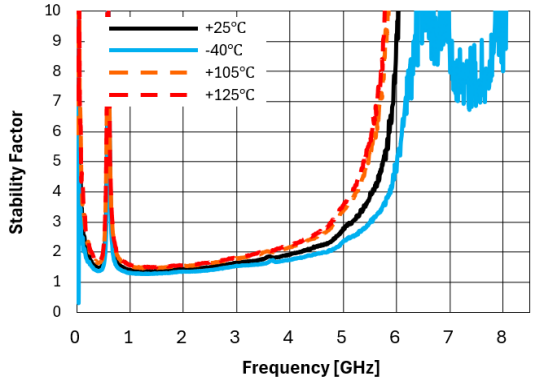



**Figure 55. OIP3 vs. Frequency vs. VDD**
Over Temperature (Max Gain State)

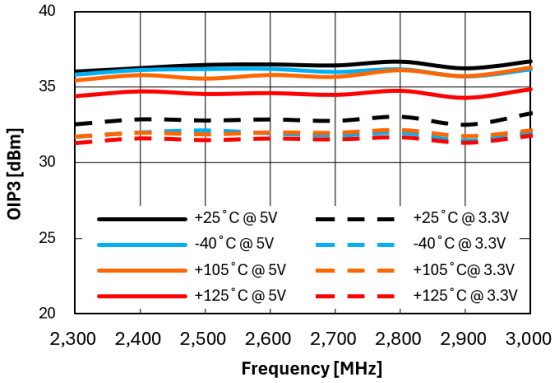



**Figure 56. OIP3 vs. Frequency vs. VDD**
Over Temperature (15.5dB Attenuation State)

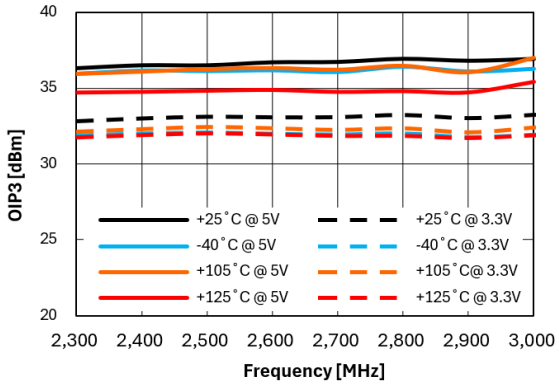



**Figure 57. P1dB vs. Frequency vs. VDD**
Over Temperature (Max Gain State)

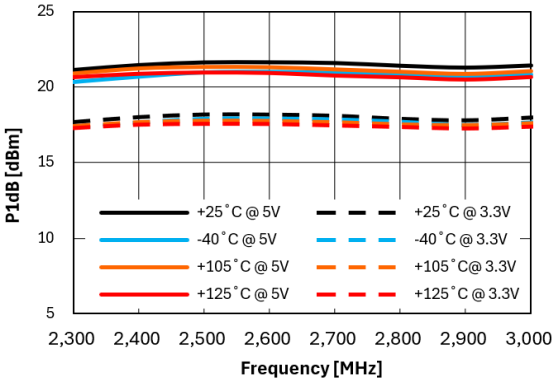



**Figure 58. Noise Figure vs. Frequency @ VDD = 5V**
Over Temperature (Max Gain State)

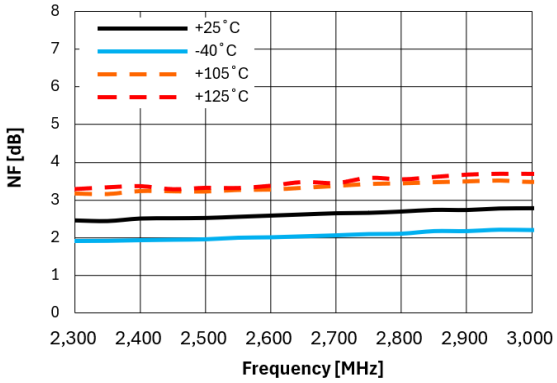
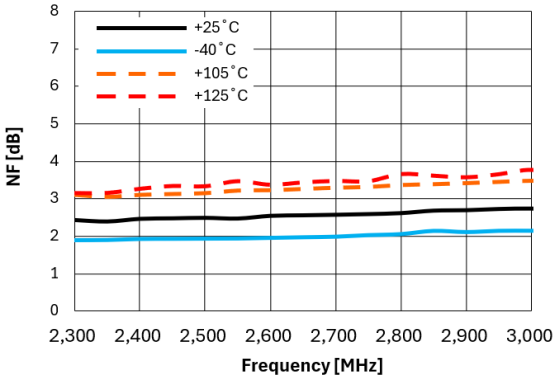



**Figure 59. Noise Figure vs. Frequency @ VDD = 3.3V**
Over Temperature (Max Gain State)



## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 2.3 ~ 3GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 18**

**Figure 60. Attenuation Error vs Frequency**
Over Major Attenuation Steps

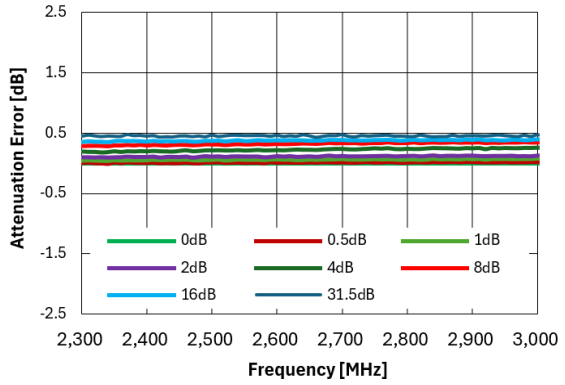



**Figure 61. Attenuation Error vs Attenuation Setting**
Over Major Frequency (Max Gain State)

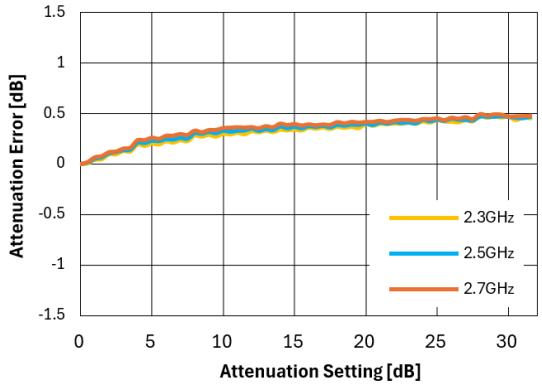



**Figure 62. Attenuation Error at 2.3GHz vs Temperature**
Over All Attenuation States

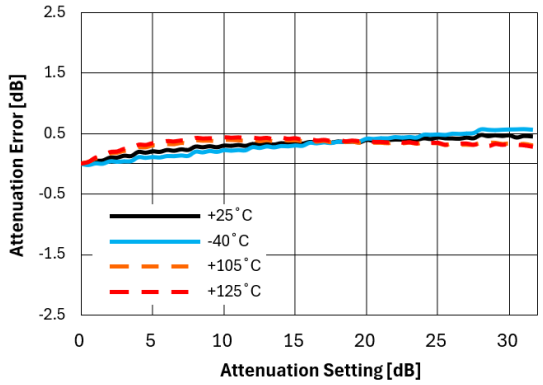



**Figure 63. Attenuation Error at 2.5GHz vs Temperature**
Over All Attenuation States

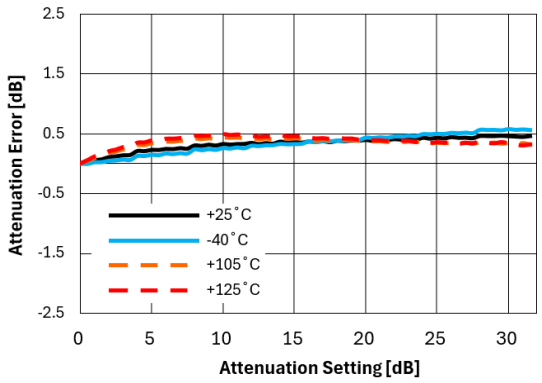
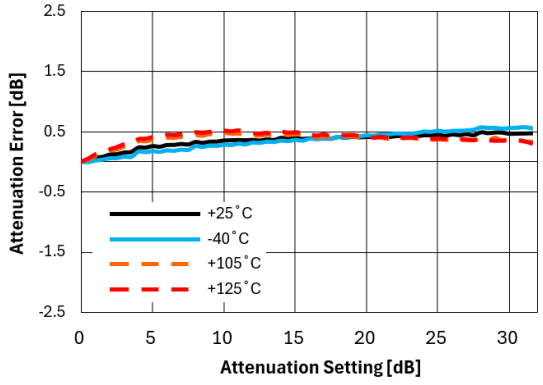


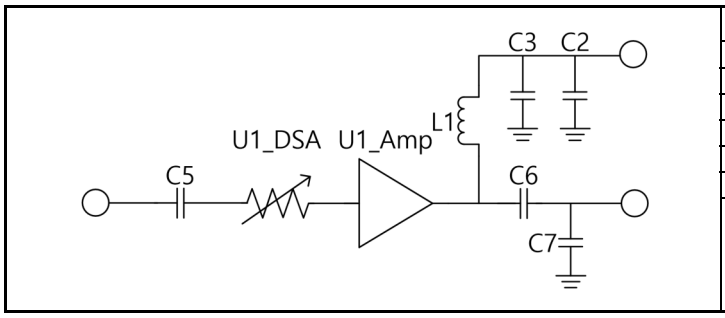

**Figure 64. Attenuation Error at 2.7GHz vs Temperature**
Over All Attenuation States



## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 3.3 ~ 4GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 21**

**Table 21. 3.3 ~ 4GHz RF Application Circuit**




| BOM | |
|---|---|
| L1 | 1nH |
| C2 | 100nF |
| C3 | 100pF |
| C5 | 100pF |
| C6 | 100pF |
| C7 | 0.5pF |

This value can be changed little by little according to the frequency band and bandwidth.

**Table 22. Typical RF Performance @ VDD = 5V**

| Parameter | Frequency | | | Unit |
|---|---|---|---|---|
| | 3300 | 3600 | 3800 | MHz |
| **Gain**[1] | 17.0 | 16.8 | 16.7 | dB |
| **S11** | -12.5 | -12.7 | -12.8 | dB |
| **S22** | -11.6 | -10.4 | -9.9 | dB |
| **OIP3**[2] | 36.6 | 36.5 | 36.7 | dBm |
| **P1dB** | 21.0 | 21.1 | 20.9 | dBm |
| **Noise Figure** | 2.8 | 2.9 | 3.1 | dB |

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 measured with two tones at an output of 3 dBm per tone separated by 1 MHz.

**Table 23. Typical RF Performance @ VDD = 3.3V**

| Parameter | Frequency | | | Unit |
|---|---|---|---|---|
| | 3300 | 3600 | 3800 | MHz |
| **Gain**[1] | 16.4 | 16.2 | 16.0 | dB |
| **S11** | -11.6 | -11.8 | -11.9 | dB |
| **S22** | -11.2 | -10.0 | -9.4 | dB |
| **OIP3**[2] | 33.7 | 32.8 | 32.6 | dBm |
| **P1dB** | 17.6 | 17.7 | 17.5 | dBm |
| **Noise Figure** | 2.8 | 3.0 | 3.0 | dB |

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 measured with two tones at an output of 3 dBm per tone separated by 1 MHz.

**Figure 65. Gain vs. Frequency @ VDD = 5V**
Over Temperature

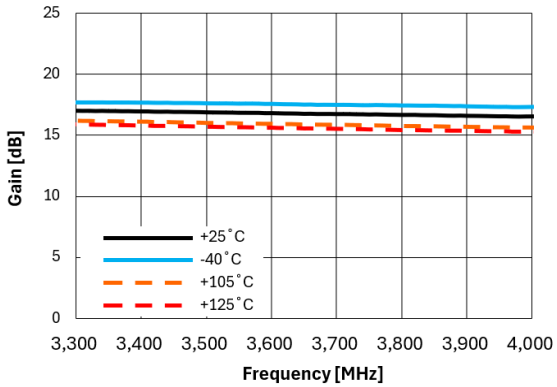
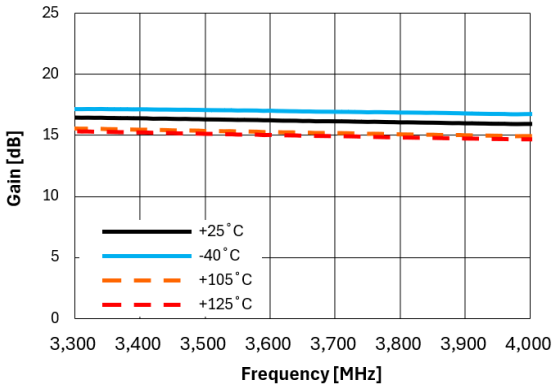



**Figure 66. Gain vs. Frequency @ VDD = 3.3V**
Over Temperature



## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 3.3 ~ 4GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 21**

**Figure 67. Gain vs. Frequency**
Over Major Attenuation States

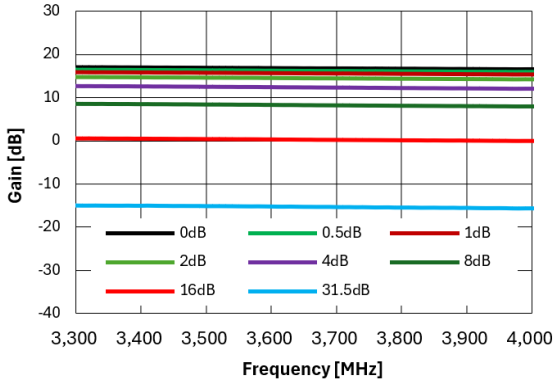



**Figure 68. Gain vs. Frequency vs VDD**
Max Gain States

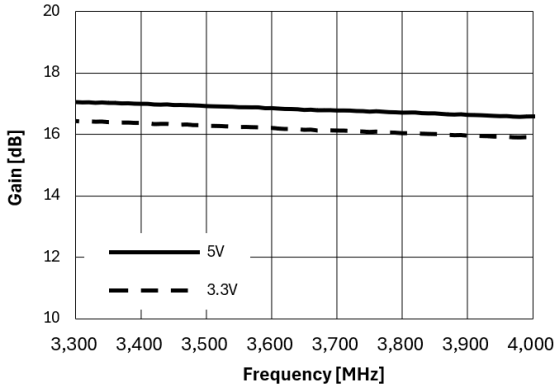



**Figure 69. Input Return Loss vs. Frequency**
Over Temperature (Min[1] / Max Gain State)

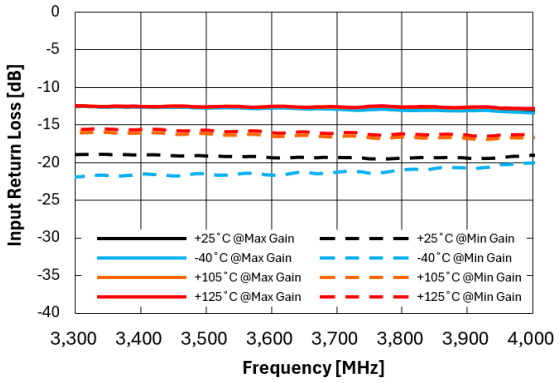
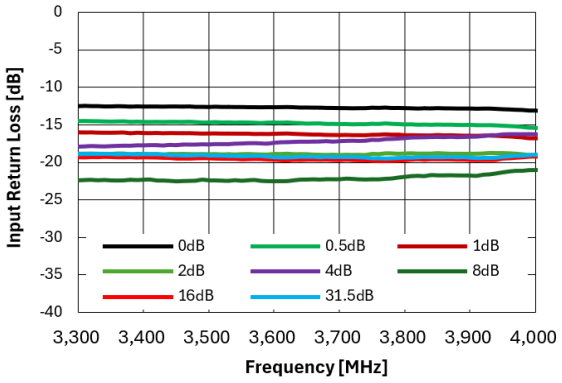



**Figure 70. Input Return Loss vs. Frequency**
Over Major Attenuation States




1.Min Gain was measured in the state is set with attenuation 31.5dB.

**Figure 71. Output Return Loss vs. Frequency**
Over Temperature (Min[1] / Max Gain State)

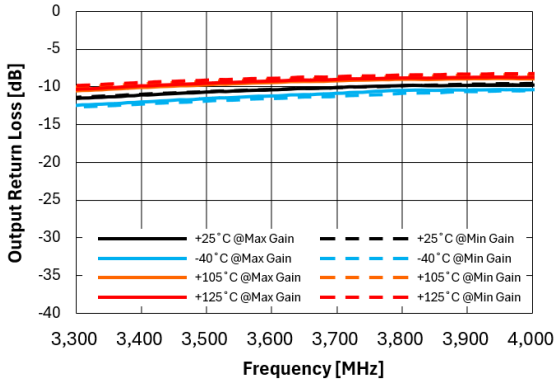
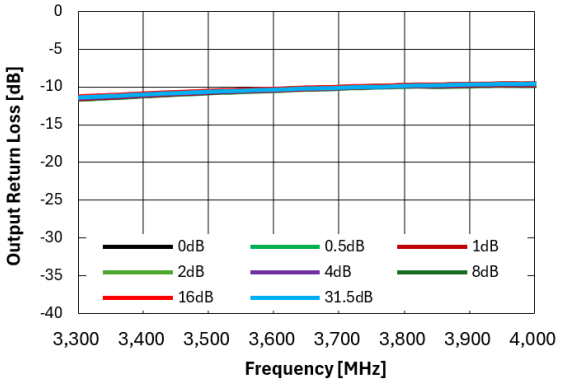



**Figure 72. Output Return Loss vs. Frequency**
Over Major Attenuation States




1.Min Gain was measured in the state is set with attenuation 31.5dB.

## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 3.3 ~ 4GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 21**

**Figure 73. K Factor vs Frequency**
Over Temperature (Max Gain State)

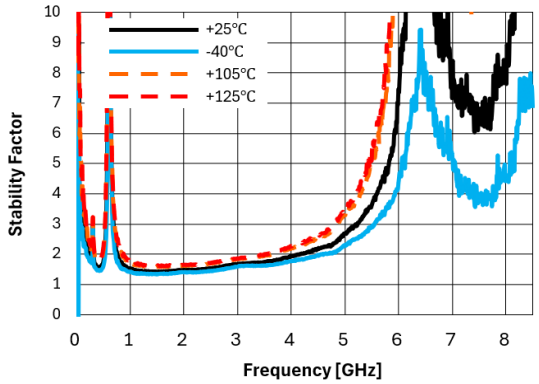



**Figure 74. OIP3 vs. Frequency vs. VDD**
Over Temperature (Max Gain State)

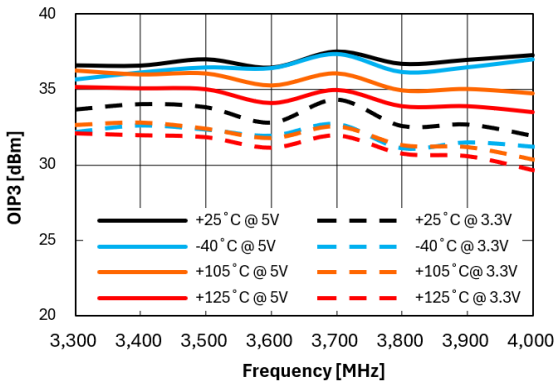



**Figure 75. OIP3 vs. Frequency vs. VDD**
Over Temperature (15.5dB Attenuation State)

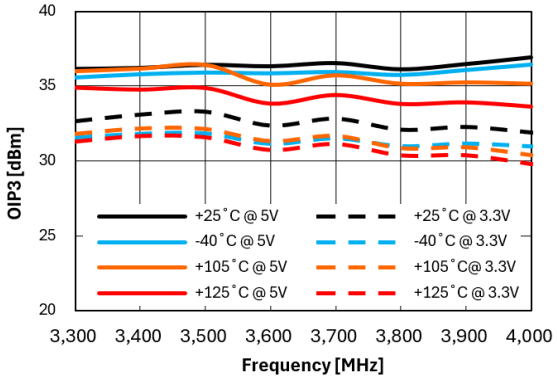



**Figure 76. P1dB vs. Frequency vs. VDD**
Over Temperature (Max Gain State)

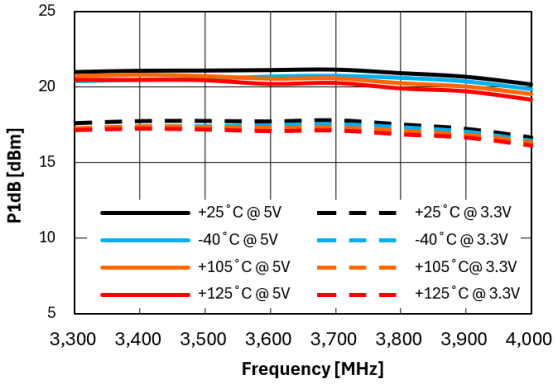



**Figure 77. Noise Figure vs. Frequency @ VDD = 5V**
Over Temperature (Max Gain State)

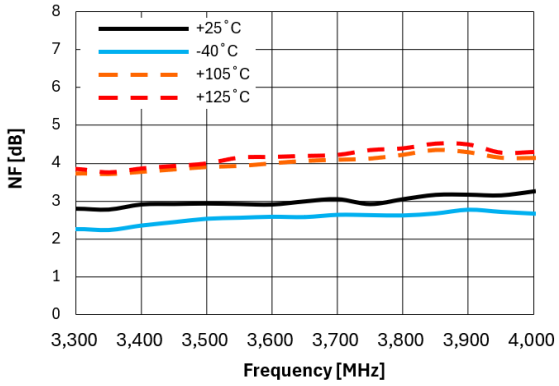
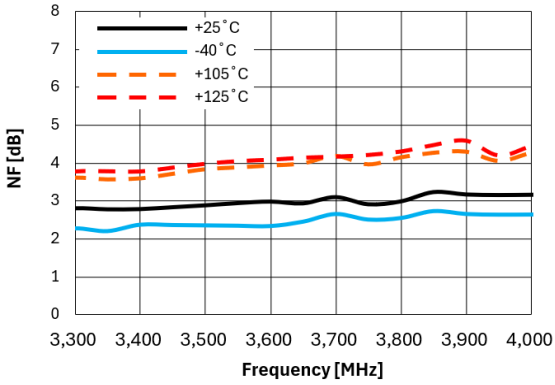



**Figure 78. Noise Figure vs. Frequency @ VDD = 3.3V**
Over Temperature (Max Gain State)



## Typical RF Performance Plot - BVA1621 EVK - PCB (Application Circuit : 3.3 ~ 4GHz)

**Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 21**

**Figure 79. Attenuation Error vs Frequency**
Over Major Attenuation Steps

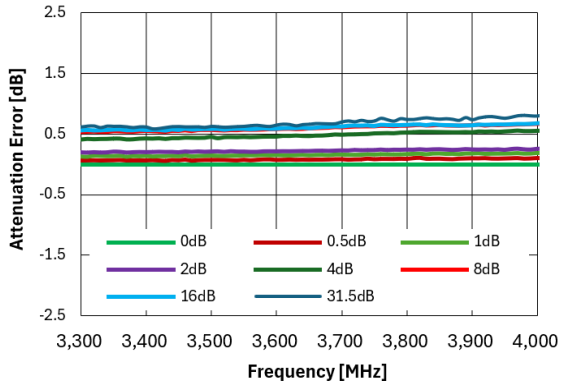



**Figure 80. Attenuation Error vs Attenuation Setting**
Over Major Frequency (Max Gain State)

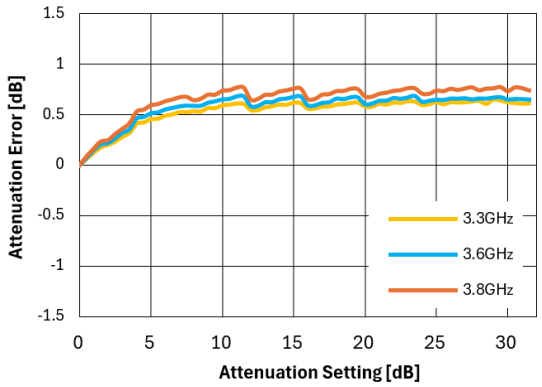



**Figure 81. Attenuation Error at 3.3GHz vs Temperature**
Over All Attenuation States

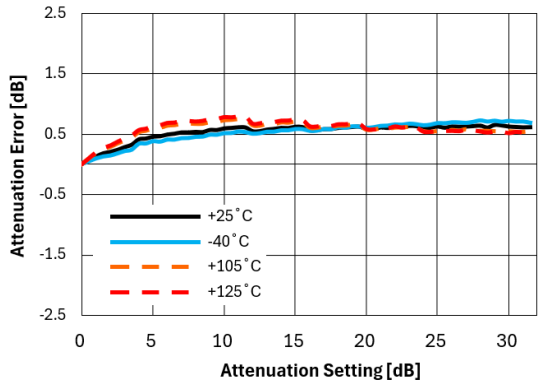



**Figure 82. Attenuation Error at 3.6GHz vs Temperature**
Over All Attenuation States

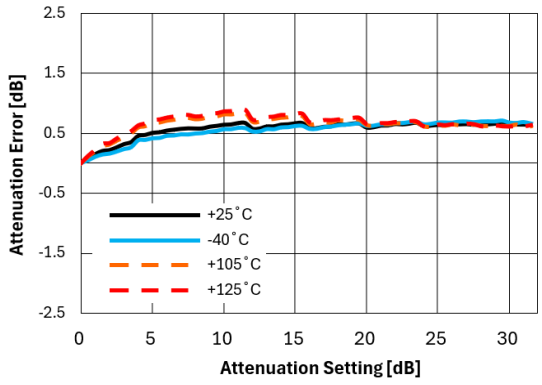



**Figure 83. Attenuation Error at 3.8GHz vs Temperature**
Over All Attenuation States

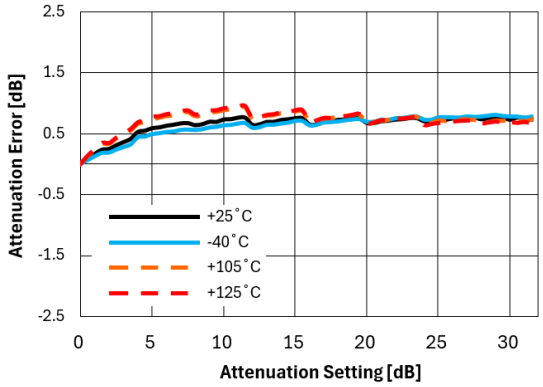


**Figure 84. Evaluation Board Schematic Diagram**

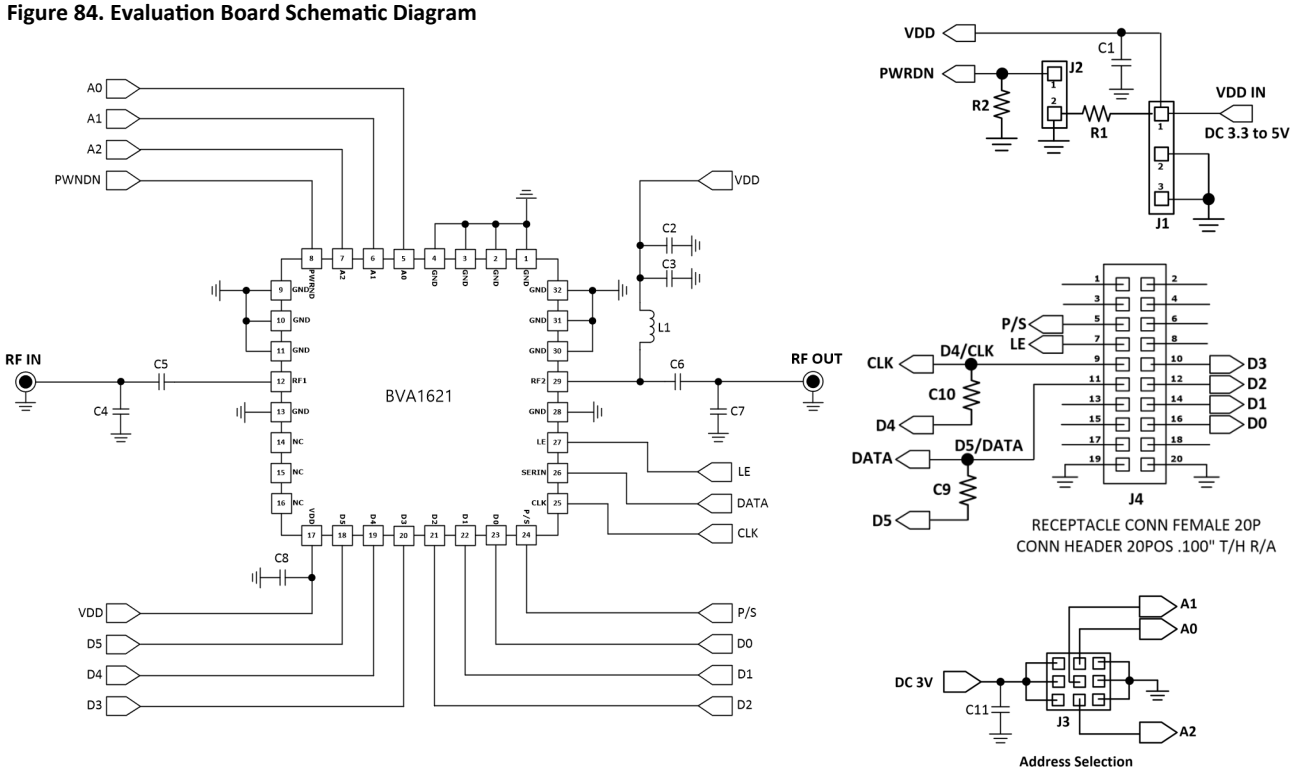



**Figure 85. BVA1621 Evaluation Board**

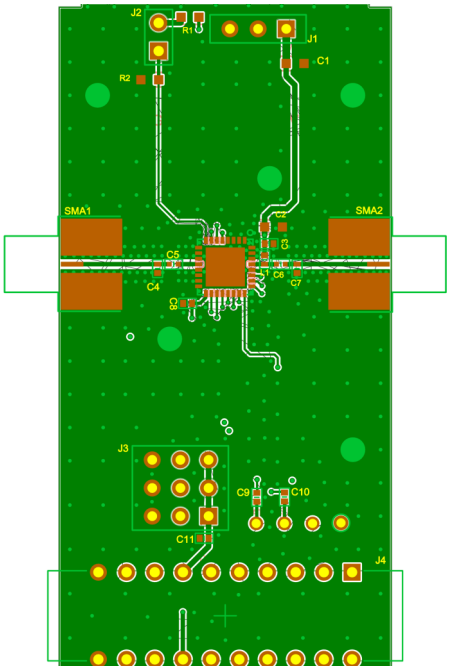



**Table 24. Application Circuit**

| Application Circuits by Frequency Range | | | | |
|---|---|---|---|---|
| Ref Des | 0.4 - 1.2GHz | 1.5 - 2.3GHz | 2.3 - 3GHz | 3.3 - 4GHz |
| L1 | 33nH | 3.3nH | 1.5nH | 1nH |
| C7 | 0.8pF | 0.7pF | 0.7pF | 0.5pF |

**Table 25. Bill of Material - Evaluation Board**

| No. | Ref Des | Qty | Part Number | REMARK |
|---|---|---|---|---|
| 1 | L1 | 1 | IND 0402 | Refer to Table 24 |
| 2 | C1 | 1 | CAP 0608 1uF | |
| 3 | C2 | 1 | CAP 0608 100nF | |
| 4 | C3, C5, C6 | 3 | CAP 0603 100pF | |
| 5 | C7 | 1 | CAP 0201 | Refer to Table 24 |
| 6 | C8, C11 | 2 | CAP 0402 100nF | |
| 7 | C9, C10 | 2 | RES 0402 1kohm | |
| 8 | R1 | 1 | RES 0608 1kohm | |
| 9 | R2 | 1 | RES 0608 30kohm | |
| 10 | U1 | 1 | BVA1621 | SIP LGA 5x5 32Lead |
| 11 | SMA1, SMA2 | 2 | SMA END LAUNCH | RF SMA Connector |
| 12 | J1 | 1 | 3pin Header | 2.54mm, male |
| 13 | J2 | 1 | 2pin Header | 2.54mm, male |
| 14 | J3 | 1 | 3pin x 3 Header array | 2.54mm, male |
| 15 | J4 | 1 | Receptacle connector 20pin | 2.54mm, female |
| 16 | C4 | 1 | NC | Not Connected |

**Figure 86. Recommended Application Circuits in Serial Mode**

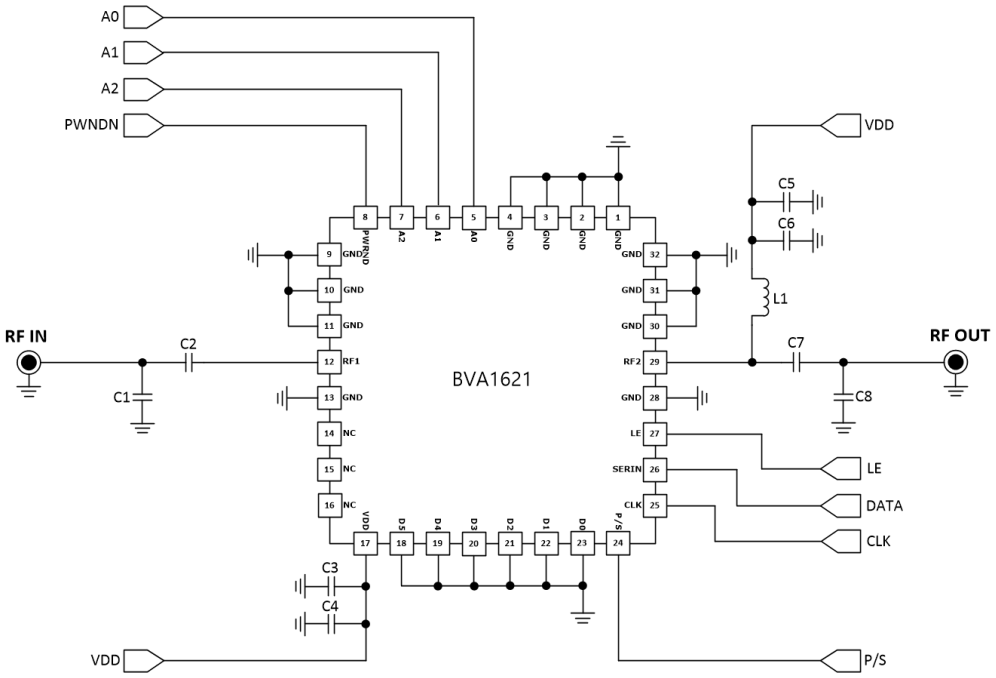



**Figure 87. Recommended Application Circuits in Parallel Mode**

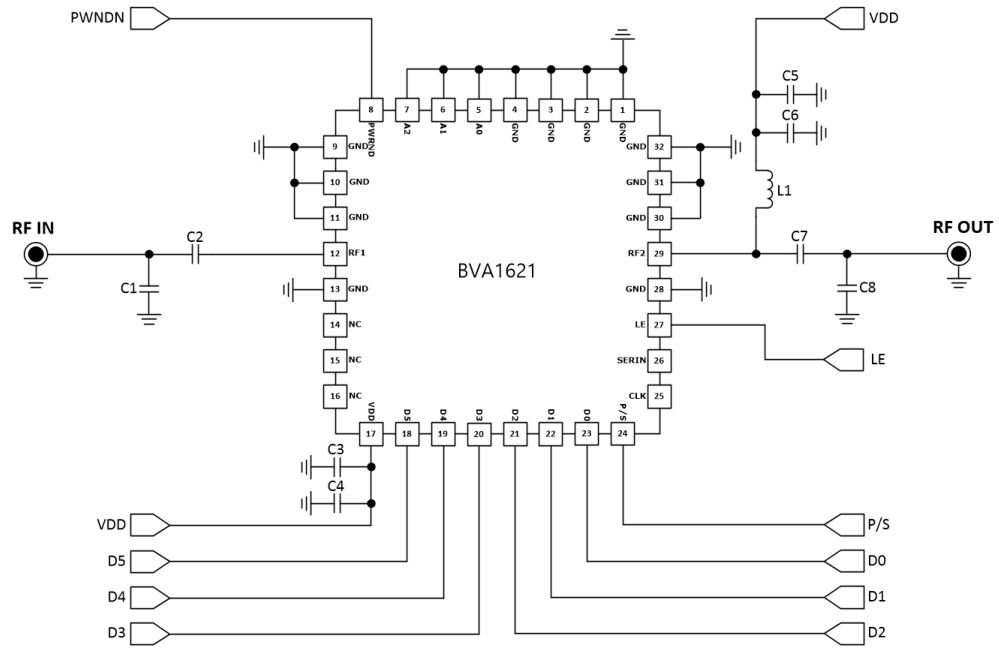


**Figure 88. Suggested PCB Land Pattern and PAD Layout**

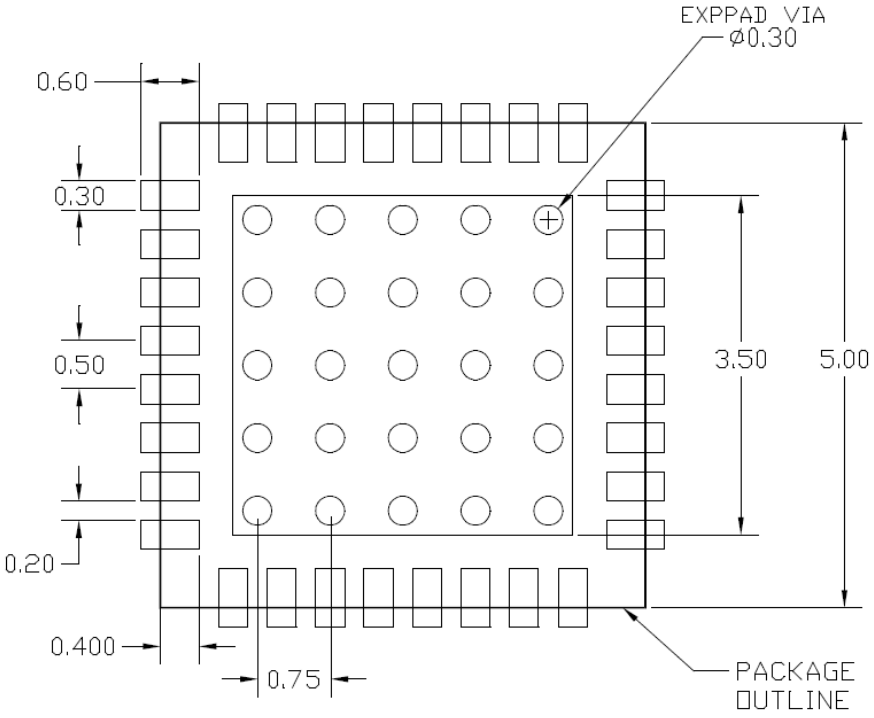



**Figure 89. Evaluation Board PCB Layer Information**

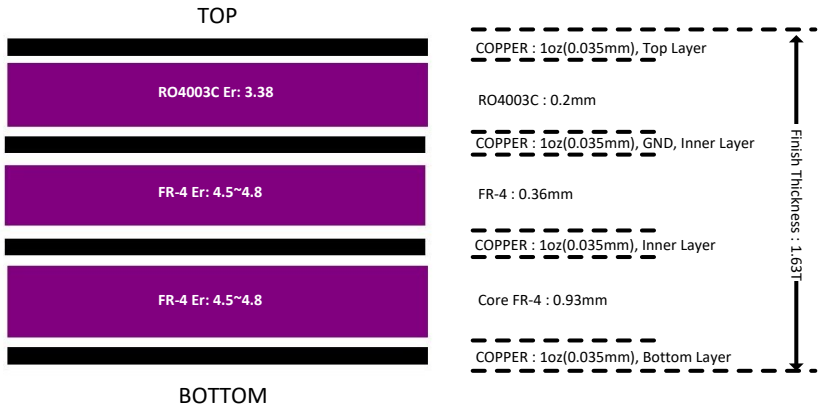
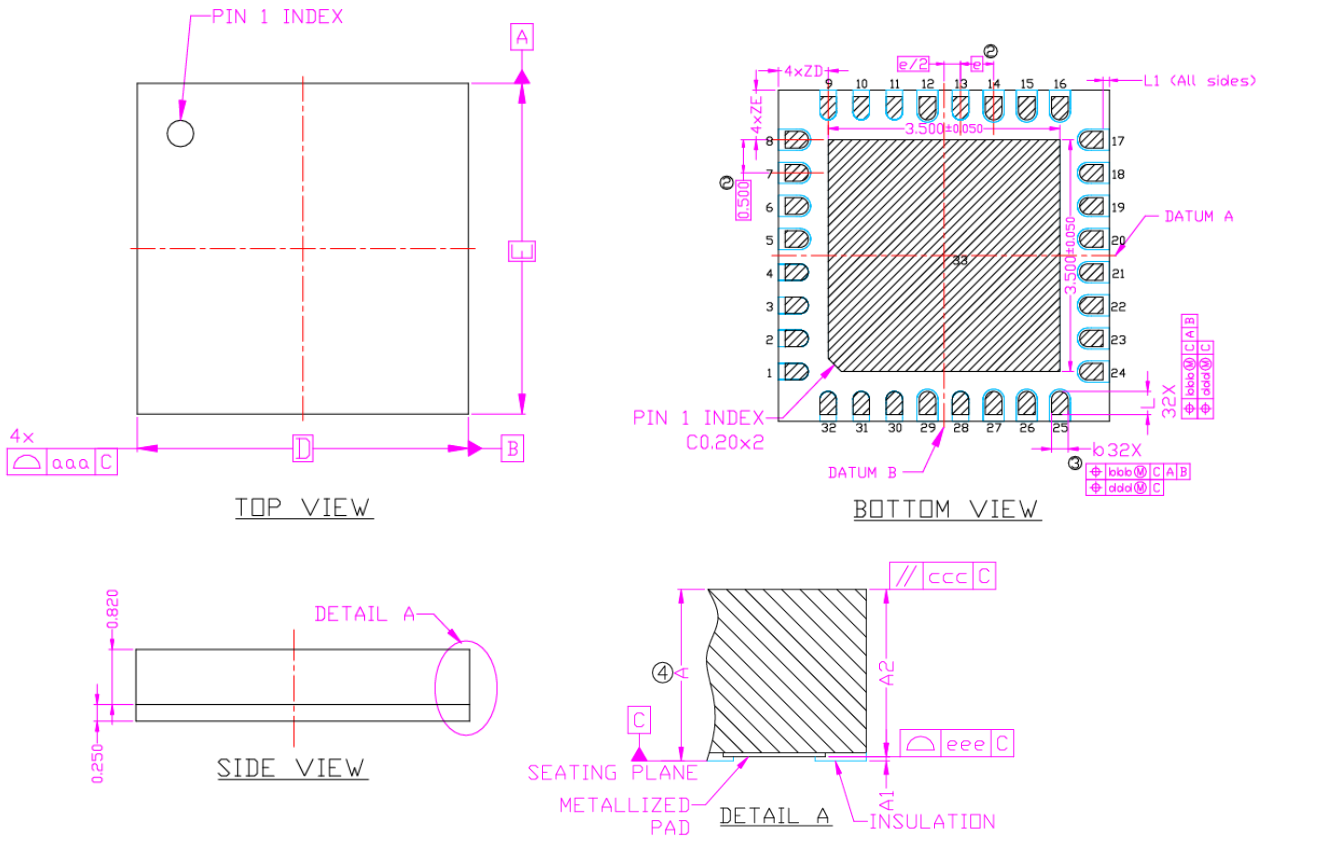


**Figure 90. Package Outline Dimension**




DIMENSIONAL REFERENCES unit: mm

| REF. | Min. | Nom. | Max. |
|---|---|---|---|
| A | 1.02 | 1.07 | 1.12 |
| A1 | – | – | 0.03 |
| A2 | – | – | 1.09 |
| b | 0.20 | 0.25 | 0.30 |
| L | 0.30 | 0.35 | 0.40 |
| D | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 |
| ZD | 0.75 BSC | | |
| ZE | 0.75 BSC | | |
| e | 0.50 BSC | | |
| L1 | 0.10 REF | | |

DIMENSIONAL REFERENCES unit: mm

| REF. | TOLERANCE OF FORM AND POSITION |
|---|---|
| aaa | 0.10 |
| bbb | 0.10 |
| ccc | 0.10 |
| ddd | 0.08 |
| eee | 0.08 |

Notes :

① ALL DIMENSION ARE IN MILLIMETER.

② 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.

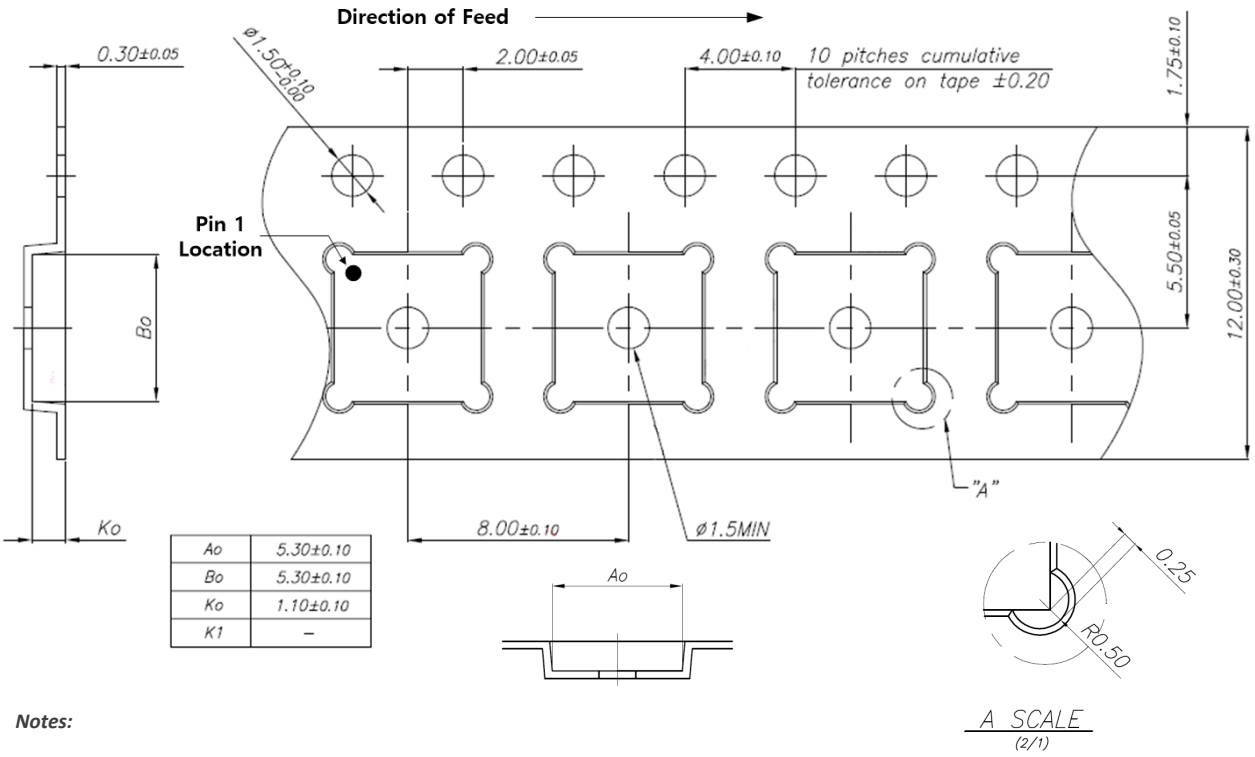
③ DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.

④ DIMENSION 'A' INCLUDES PACKAGE WARPAGE.

⑤ EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.

⑥ PACKAGE DIMENSIONS TAKE REFERENCE TO JEDEC MO-208 REV.C.

**Figure 91. Tape & Reel**




| | |
|---|---|
| Ao | 5.30±0.10 |
| Bo | 5.30±0.10 |
| Ko | 1.10±0.10 |
| K1 | – |

*Notes:*

1. *10 sprocket hole pitch cumulative tolerance 0.2/-0.2*
2. *Camber not to exceed 1mm in 250mm.*
3. *Material : Black conductive Polystyrene.*
4. *Ao and Bo measured on a plane 0.3mm above the bottom of the pocket*
5. *Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.*
6. *Pocket center position relative to sprocket hole center measured as true position center of pocket, not pocket hole center.*
7. *Pocket center and pocket hole center must be same position.*

| Packaging information: | |
|---|---|
| Tape Width | 12mm |
| Reel Size | 7" |
| Device Cavity Pitch | 8mm |
| Devices Per Reel | 1K |

**Figure 92. Package Marking**


| Marking information: | |
|---|---|
| BVA1621 | Device Name |
| YY | Year |
| WW | Work Week |
| XX | Wafer Run Number |

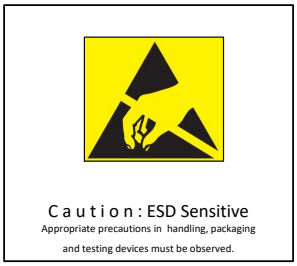
### Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

### MSL / ESD Rating

| | |
|---|---|
| **ESD Rating:** | Class 1C |
| **Value:** | ±1000V |
| **Test:** | Human Body Model (HBM) |
| **Standard:** | JEDEC Standard JS-001-2017 |
| | |
| **ESD Rating:** | Class C3 |
| **Value:** | ±1000V |
| **Test:** | Charged Device Model (CDM) |
| **Standard:** | JEDEC Standard JS-002-2018 |
| | |
| **MSL Rating:** | **Level 3 at +260°C convection reflow** |
| **Standard:** | JEDEC Standard J-STD-020 |




Proper ESD procedures should be followed when handling this device.

## RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

### NATO CAGE code:

| | | | | |
|---|---|---|---|---|
| 2 | N | 9 | 6 | F |