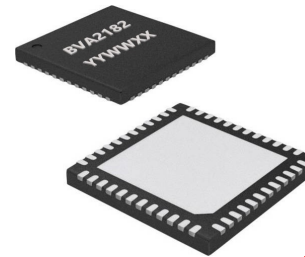


Device Features

- 48Pin 7 x 7 x 0.9mm QFN Package
- Integrates Amp1(Gain Block), DSA1 ,DSA2 Amp2(Gain Block) Functionality
- Wide Power supply range of +2.7~5.5V(DSA1,2)
- Single Fixed +5.0V supply (Amp1,2)
- 0.5-3.8GHz Broadband Performance
- 33.4dB Gain at 1.9GHz (with 3dB Pad in Application Circuit)
- 1.6dB Noise Figure at max gain setting at 1.9GHz
- 21.2dBm P1dB at 1.9GHz
- 38.2dBm OIP3 at 1.9GHz(5dBm per tone)
- Attenuation: 0.5 dB steps to 31.5 dB
- Safe attenuation state transitions
- Monotonicity: 0.5 dB up to 4 GHz
- High attenuation accuracy (DSA to Amp)
±(0.15dB + 3% x ATT setting) @ 1.7~2.2GHz
- 1.8V control logic compatible
- Programming modes
- Serial
- Unique power-up state selection
- Two Functions application which are Dual channel Application (Tx-Rx) or Single Channel Application(2stage Amp and 2stage DSA)
- Lead-free/RoHS2-compliant QFN SMT Package



48-lead 7mm x 7mm x 0.9mm QFN

Figure 1. Package Type

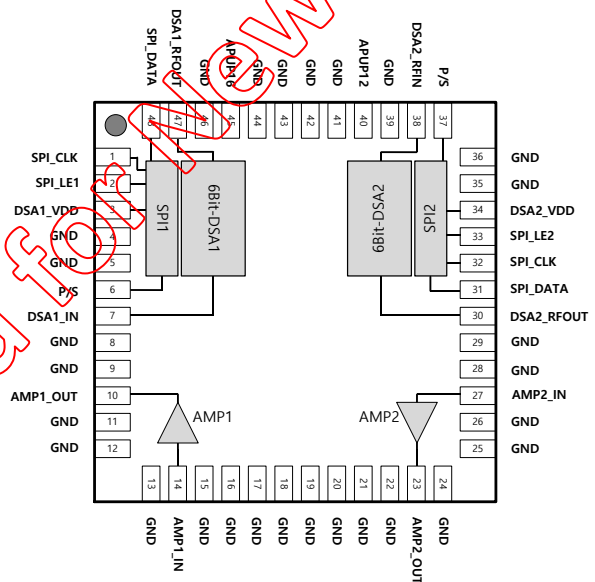


Figure 2. Functional Block Diagram

Product Description

The BVA2182 is a digitally controlled variable gain amplifier (DVGA) in a 7x7mm QFN package, with a broadband frequency range of 0.5GHz to 3.8GHz and an operating V_{DD} of 5.0V at 170mA.

BVA2182 is high performance and high dynamic range makes it ideally suited for use in WCDMA/LTE wireless infrastructure point-to-point and other demanding wireless applications.

The BVA2182 is an integration of two high performance digital 6-step attenuator (DSA) that provides a 31.5 dB attenuation range in 0.5 dB steps, and high linearity broadband gain block amplifiers featuring high ACLR and P1.

The BVA2182 digital control interface supports serial programming of the attenuator, and includes the ability to define the initial attenuation state at power-up.

The BVA2182 is integrated of two gain blocks (AMP1, AMP2), a digital step attenuator(DSA1,DSA2). Implementation requires only a few external components, such as DC blocking capacitors on the Input and Output pins, plus a bypass capacitor and a RF choke for the Output port. The BVA2182 is composed of Amp1 + DSA1 + DSA2 + Amp2. In some case, It can be use with a dual path such as Amp1 + DSA1 and DSA2 + Amp2 .

Application

- Base station/Repeater Infrastructure
- LTE/WCDMA/CDMA Wireless infrastructure and other high performance RF application
- Commercial/Industrial/Military Wireless system
- General purpose Wireless

DUAL DIGITAL VARIABLE GAIN AMPLIFIER

0.5GHz — 3.8GHz

Table 1. Electrical Specifications¹

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			500		3800	MHz
Gain		ATT = 0dB, at 1900MHz		33.5		dB
Attenuation Control range		0.5dB step		0.31.5		dB
Attenuation Step				31.5		dB
Attenuation Accuracy	>0.6GHz-1GHz	Any bit or bit combination	±(0.15dB + 2% of ATT setting)			dB
	>1.6GHz-2.2GHz		±(0.15dB + 3% of ATT setting)			
	>2.2GHz-2.8GHz		±(0.15dB + 5% of ATT setting)			
	>3.3GHz-3.8GHz		±(0.15dB + 10% of ATT setting)			
Return loss (input or output port)	Input Return Loss	ATT = 0dB		15.8		dB
	Output Return Loss			18.7		
Output Power for 1dB Compression		ATT = 0dB, at 1900MHz		21.2		dBm
Output Third Order Intercept Point		ATT = 0dB, at 1900MHz Pout= +5dBm/tone Δf = 1MHz.		38.2		dBm
Noise Figure		ATT = 0dB, at 1900MHz		1.6		dB
Switching time		50% CTRL to 90% or 10% RF		500	800	ns
Supply voltage		DSA	2.7		5.5	V
		AMP		5		V
Supply Current		AMP1 + DSA1 + DSA2 + AMP2		170		mA
Control Interface		Serial mode		6		Bit
Impedance				50		Ω

1. Device performance _ measured on a BeRex evaluation board at 25°C, 50 Ω system, VDD=+5.0V, measure on Evaluation Board (AMP1 + DSA1 + DSA2 + AMP2)

2. Gain measured with a Pi 3dB Pad in Application circuit on Evaluation board

DUAL DIGITAL VARIABLE GAIN AMPLIFIER

0.5GHz — 3.8GHz

Table 2. Typical RF Performance¹

Parameter	Frequency												Unit
	Low Band Application (0.6-1GHz)			Medium Band Application (1.7-2.2GHz)			High Band Application (2.3-2.8GHz)			High Band Application (3.3-3.8GHz)			
	0.6	0.8	1	1.7	1.95	2.2	2.3	2.55	2.8	3.3	3.5	3.8	GHz
Gain	33.5	33.3	32.7	33.9	33.5	32.4	33.5	33.1	32	32	30.8	30.2	dB
S11	-16.1	-17	-15.2	-14.3	-15.8	-11.2	-13.3	-16.9	-17	-15.3	-21.3	-29.3	dB
S22	-26.2	-40	-38.7	-14	-18.7	-24.9	-17.9	-18.7	-15.9	-10	-7.7	-6.5	dB
OIP3	37.8	38.1	37.7	38.1	38.2	38.4	38	38.2	38.4	37.5	38.7	39.2	dBm
P1dB	21.3	21.4	21.5	21.3	21.2	21.2	20.6	20.8	20.3	19.2	18.9	18.4	dBm
N.F	1.4	1.3	1.5	1.3	1.6	1.8	1.7	1.7	1.8	2	2.2	2.4	dB

1. Device performance_ measured on a BeRex evaluation board at 25°C, V_{DD}=+5.0V, 50 Ω system. measure on Evaluation Board (DSA to AMP)

2. OIP3_ measured with two tones at an output of +5 dBm per tone separated by 1 MHz.

3. Gain measured with a 7dB,3dB,2dB pi Pad in Application circuit on Evaluation board .(refer to table 11,13,15)

Table 3. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage(V _{DD})	MCM(AMP1+DSA1+DSA2+AMP2)	-0.3		5.5	V
Supply Current	MCM(AMP1+DSA1+DSA2+AMP2)			380	mA
Digital input voltage	DSA	-0.3		3.6	V
Maximum input power	MCM(AMP1+DSA1+DSA2+AMP2)			+20	dBm
Storage Temperature	MCM(AMP1+DSA1+DSA2+AMP2)	-55		150	°C
Junction Temperature	MCM(AMP1+DSA1+DSA2+AMP2)			220	°C

Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Bandwidth	MCM(AMP1+DSA1+DSA2+AMP2)	500		3800	MHz
Supply Voltage(V _{DD})	MCM(AMP1,AMP2)		5		V
	MCM(DSA1,DSA2)	2.7		5.5	V
Control Voltage	Digital input high	1.17		3.6	V
	Digital input low	-0.3		0.6	V
I _c @ (V _{DD} =5V)	MCM(AMP1+DSA1+DSA2+AMP2)		170		mA
Operating Temperature	MCM(AMP1+DSA1+DSA2+AMP2)	-40		105	°C

DUAL DIGITAL VARIABLE GAIN AMPLIFIER

0.5GHz — 3.8GHz

Programming Options

BVA2182 can be programmed using serial interface. Serial mode is P/S Pin pulling it to a voltage logic High.

Serial Control Mode

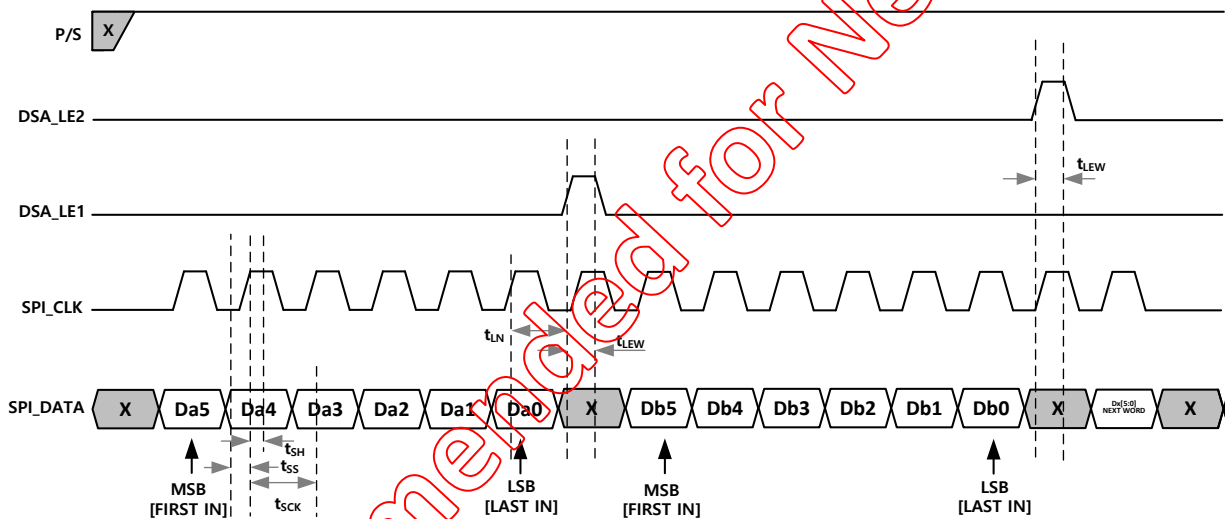
The serial interface is a 6 bit shift register to shift in the data MSB (Da5,Db5) first. It is controlled by three CMOS-compatible signals: SPI_DATA, SPI_Clock, and Latch Enable (DSA_LE1, DSA_LE2). DSA1 and DSA2 can operate independently and can be controlled at the same time through single SPI_DATA and single SPI_CLOCK.

Table 5. 6-Bit Serial Word Sequence

Da5	DSA1 Attenuation 16dB Control Bit
Da4	DSA1 Attenuation 8dB Control Bit
Da3	DSA1 Attenuation 4dB Control Bit
Da2	DSA1 Attenuation 2dB Control Bit
Da1	DSA1 Attenuation 1dB Control Bit
Da0	DSA1 Attenuation 0.5dB Control Bit

Db5	DSA2 Attenuation 16dB Control Bit
Db4	DSA2 Attenuation 8dB Control Bit
Db3	DSA2 Attenuation 4dB Control Bit
Db2	DSA2 Attenuation 2dB Control Bit
Db1	DSA2 Attenuation 1dB Control Bit
Db0	DSA2 Attenuation 0.5dB Control Bit

Figure 3. Serial Mode Resister Timing Diagram



The BVA2182 has a 4-wire serial peripheral interface (SPI): serial data input (SPI_DATA), clock (SPI_CLK), and latch enable (LE1, LE2). The serial control interface is activated when P/S is set to HIGH.

In serial mode, the 6-bit Data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggled High to latch the new attenuation state into the device. LE must be set to low to clock new 6-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept High (see Figure 3 and Table 8).

Table 6. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{CLK}	Serial data clock frequency			10	MHz
t_{SCK}	Minimum serial period	70			
t_{SS}	Serial Data setup time	10			
t_{SH}	Serial Data hold time	10			
t_{LN}	LE setup time	10			
t_{LEW}	Minimum LE pulse width	30			
t_{LES}	Minimum LE pulse spacing		600		

Table 7. Mode Selection

P/S	Control Mode
LOW	Parallel
HIGH	Serial

DUAL DIGITAL VARIABLE GAIN AMPLIFIER

0.5GHz — 3.8GHz

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 0.6-1GHz)

Typical Performance Data @ 25°C and AMP_V_{DD} = 5V, DSA_V_{DD} = 3.3V unless otherwise noted and Application Circuit refer to Table 11.

Table 11. Application Circuit : 0.6 - 1GHz

Schematic Diagram		BOM		Remark
Ref	Size	Value		
C3	0402	15nH		
C2	0402	200pF		
L2	0402	33nH		
C25	0402	200pF		
C22	0402	NC		
C23	0402	100pF		
C24	0402	1uF		
C16	0402	200pF		
C15	0402	43 ohm		7dB Pad
C17	0402	130 ohm		
C18	0402	130 ohm		
C14	0402	200pF		
C11	0402	15nH		
C9	0402	200pF		
C10	0402	NC		
L1	0402	33nH		
C37	0402	200pF		
C7	0402	100pF		
C8	0402	1uF		
C20	0402	68pF		LC Filter
L4	0402	100nH		
C19	0402	22pF		LC Filter
C12	0402	22pF		
L3	0402	100nH		
C13	0402	68pF		
R15	0402	0 ohm		
C44	0402	NC		
R8	0402	0 ohm		
R9	0402	10k ohm		
R10	0402	10k ohm		
R11	0402	0 ohm		
R14	0402	0 ohm		
R13	0402	10k ohm		
R12	0402	10k ohm		
C41	0402	100pF		
C42	0402	100pF		
C45	0402	NC		

NOTE: C1,C38 is 0ohm or Copper
Any other Ref.Des(Power Supply Block), refer to table 19.

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 0.6-1GHz)

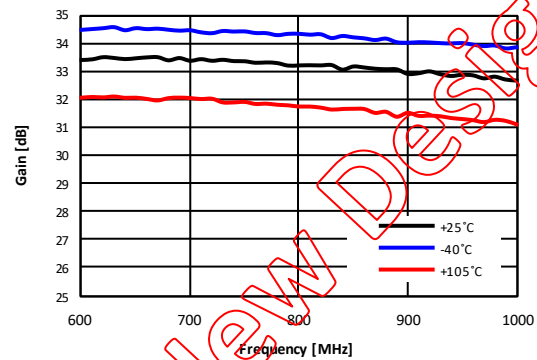
Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 11.

Table 12. Typical RF Performance

parameter	Typical Performance			Units
	0.6	0.8	1.0	
Frequency	0.6	0.8	1.0	GHz
Gain ¹	33.5	33.3	32.7	dB
S11	-16.1	-17.0	-15.2	dB
S22	-26.2	-40.0	-38.7	dB
OIP3 ²	37.8	38.1	37.7	dBm
P1dB	21.3	21.4	21.5	dBm
Noise Figure	1.4	1.3	1.5	dB

1. Gain measured with 7dB Attenuation pi Pad between DSA1 and DSA2(Refer to Table11)
 2. OIP3 measured with two tones at an output of 5 dBm per tone separated by 1 MHz.

Figure 5. Gain vs. Frequency
 over Temperature(DSA1,2 Att setting 0dB)



*Gain measured with 7dB Attenuation pi Pad between DSA1 and DSA2(Refer to Table11)

Figure 6. Gain vs Attenuation Settings
 over Major Attenuation Setting(DSA1 Att Control, DSA2 Att setting 0dB)

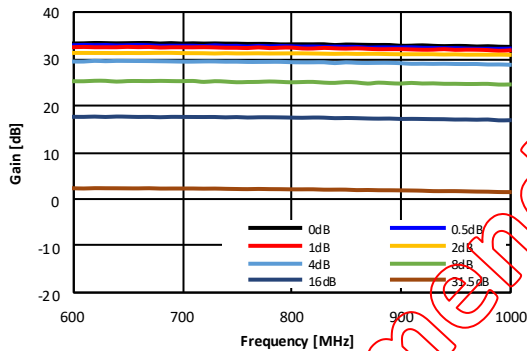


Figure 7. Gain vs Attenuation Settings
 over Major Attenuation Setting(DSA2 Att Setting 0dB, DSA1 Att Control)

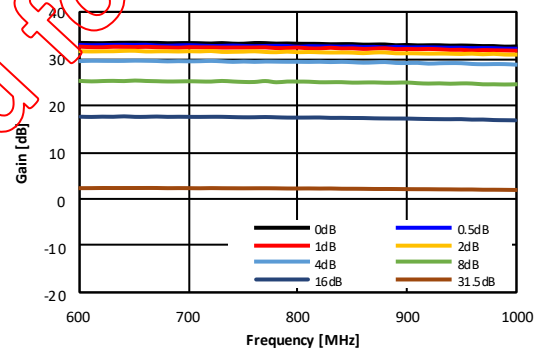
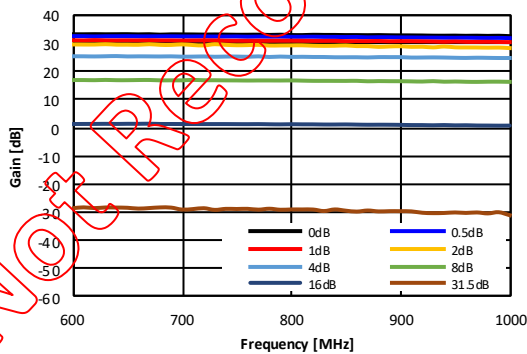


Figure 8. Gain vs Attenuation Settings
 over Major Attenuation Setting(DSA1, DSA2 DUO Att Control, Attsettingx2)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 0.6-1GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 11.

Figure 9. Input Return Loss vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)

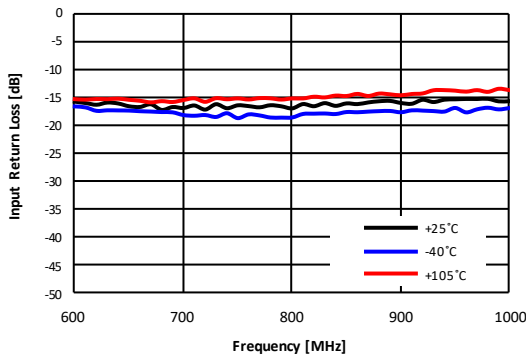


Figure 10. Input Return Loss vs Frequency
over Temperature(DSA1, DSA2 DUO Att Control, Attsetting 31.5dB)

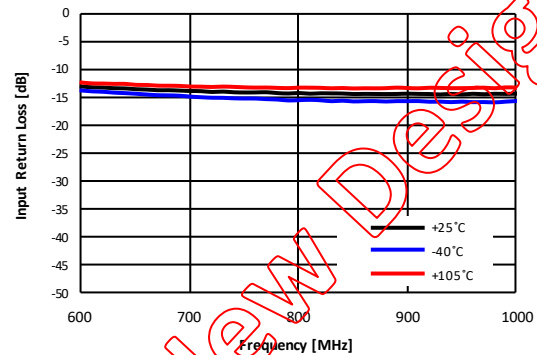


Figure 11. Input Return Loss vs Frequency
over Major Attenuation Setting(DSA1 Att Control, DSA2 Att Setting 0dB)

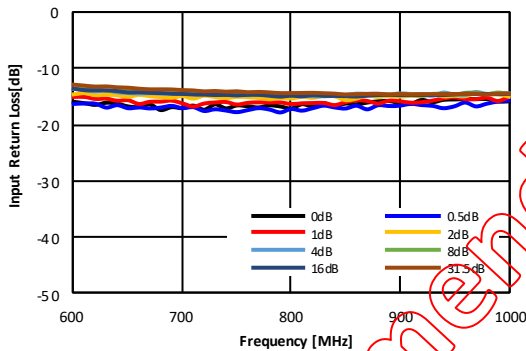


Figure 12. Input Return Loss vs Frequency
over Major Attenuation Setting(DSA2 Att Control, DSA1 Att Setting 0dB)

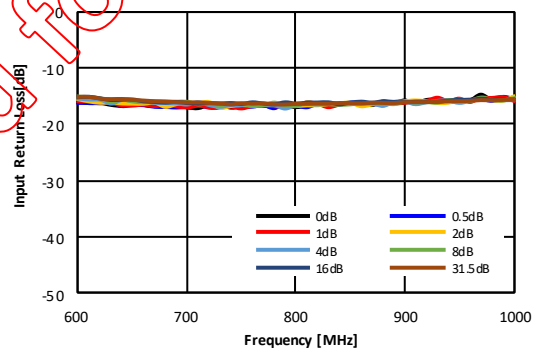


Figure 13. Output Return Loss vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)

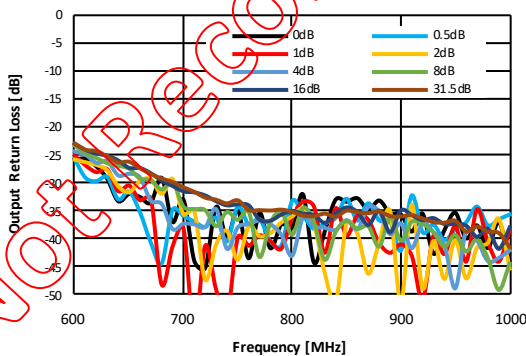
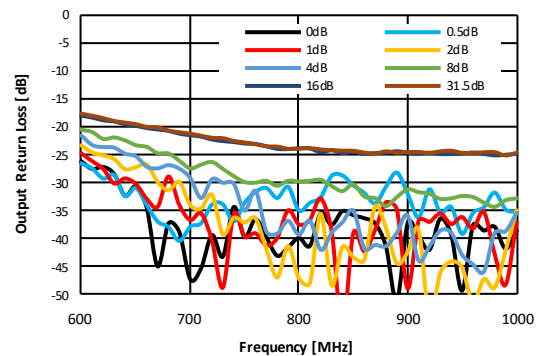


Figure 14. Output Return Loss vs Frequency
over Temperature(DSA1, DSA2 DUO Att Control, Attsetting 31.5dB)



DUAL DIGITAL VARIABLE GAIN AMPLIFIER

0.5GHz — 3.8GHz

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 0.6-1GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 11.

Figure 15. Output Return Loss vs Frequency
over Major Attenuation Setting(DSA1 Att Control, DSA2 Att Setting 0dB)

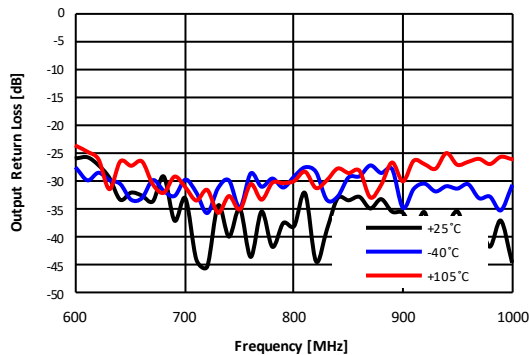


Figure 16. Output Return Loss vs Frequency
over Major Attenuation Setting(DSA2 Att Control, DSA1 Att Setting 0dB)

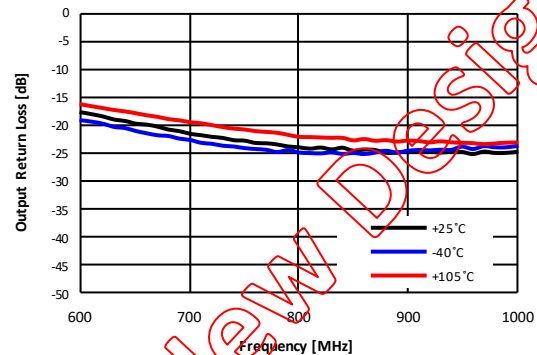


Figure 17. OIP3 vs Output Power
over Temperature(@0.6GHz, DSA1,2 Att Setting 0dB)

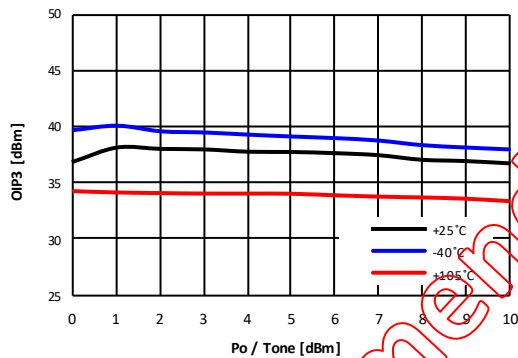


Figure 18. OIP3 vs Output Power
over Temperature(@0.8GHz, DSA1,2 Att Setting 0dB)

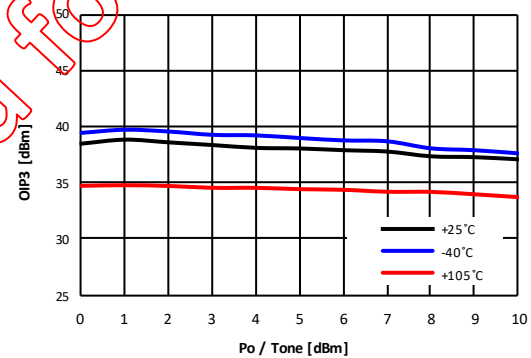


Figure 19. OIP3 vs Output Power
over Temperature(@1GHz, DSA1,2 Att Setting 0dB)

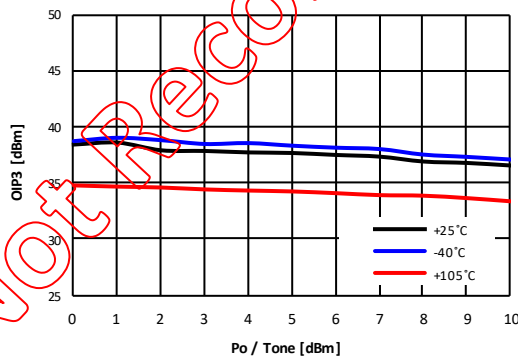
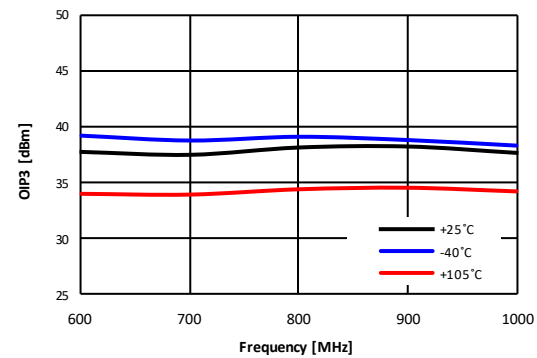


Figure 20. OIP3 vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 0.6-1GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 11.

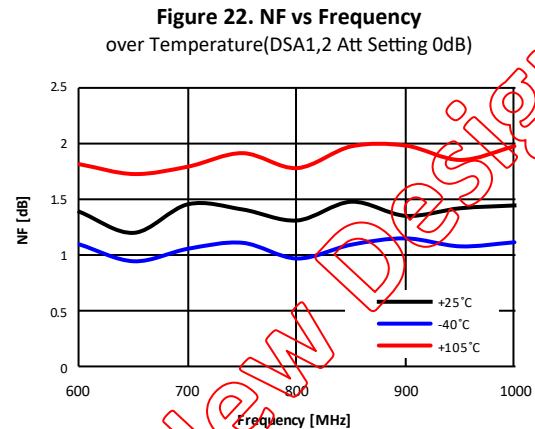
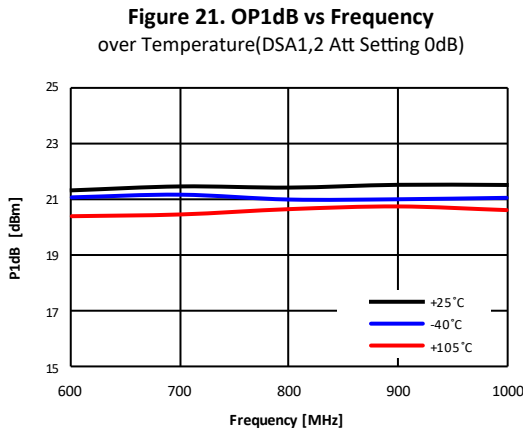


Figure 23. Attenuation Error vs Frequency
over Major Attenuation Setting(DSA1 Control, DSA2 Att Setting 0dB @+25°C)

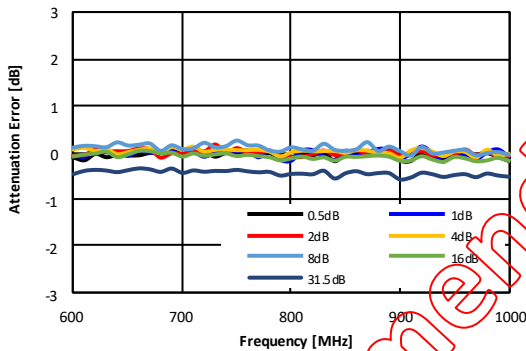


Figure 24. Attenuation Error vs Frequency
over Major Attenuation Setting(DSA2 Control, DSA1 Att Setting 0dB @+25°C)

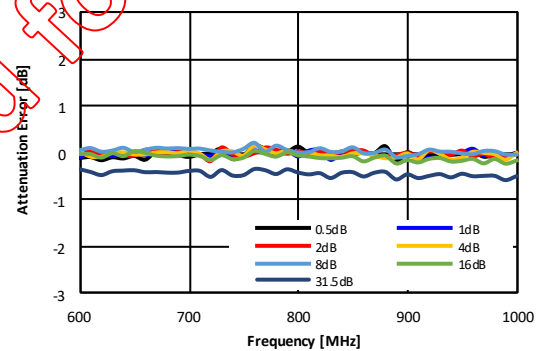


Figure 25. Attenuation Error vs Attenuation Setting
over Major Frequency(DSA1 Control, DSA2 Att Setting 0dB)

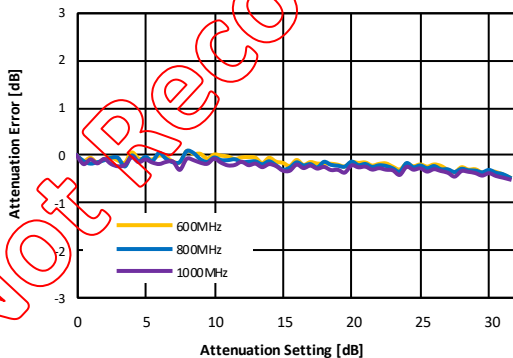
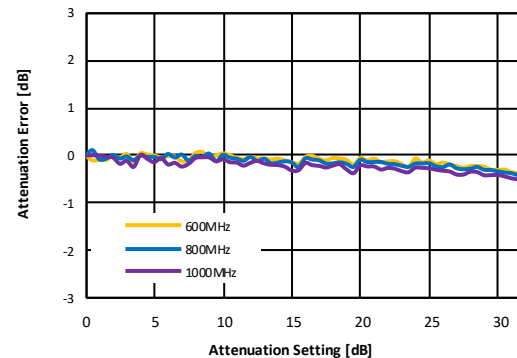


Figure 26. Attenuation Error vs Attenuation Setting
over Major Frequency(DSA2 Control, DSA1 Att Setting 0dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 0.6-1GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 11.

Figure 27. Attenuation Error vs Attenuation Setting over Temperature (@0.6GHz, DSA1 Control, DSA2 Att Setting 0dB)

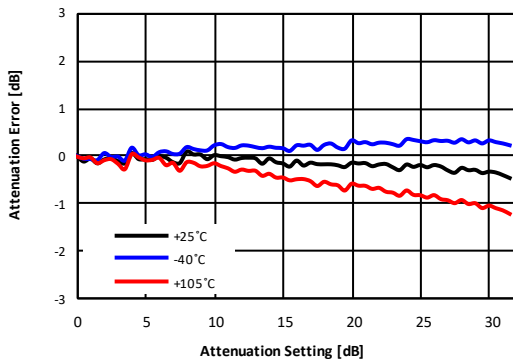


Figure 28. Attenuation Error vs Attenuation Setting over Temperature (@0.6GHz, DSA2 Control, DSA1 Att Setting 0dB)

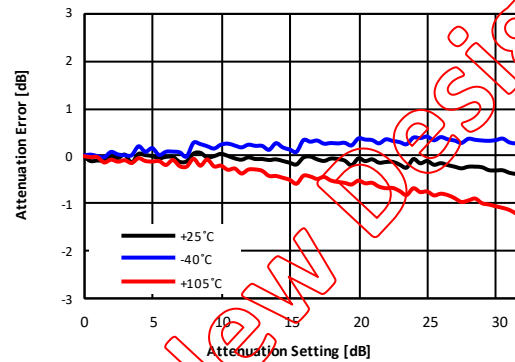


Figure 29. Attenuation Error vs Attenuation Setting over Temperature (@0.8GHz, DSA1 Control, DSA2 Att Setting 0dB)

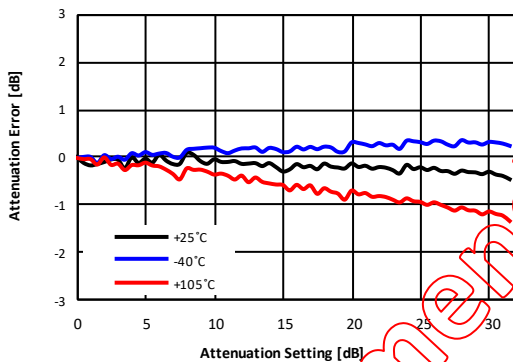


Figure 30. Attenuation Error vs Attenuation Setting over Temperature (@0.8GHz, DSA2 Control, DSA1 Att Setting 0dB)

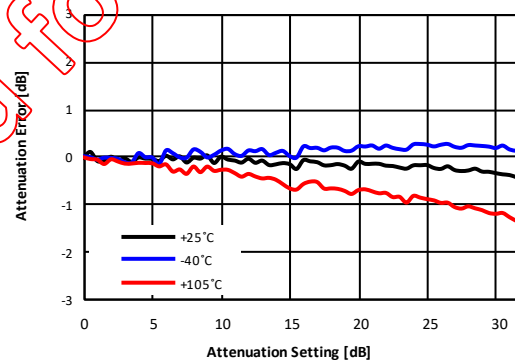


Figure 31. Attenuation Error vs Attenuation Setting over Temperature (@1GHz, DSA1 Control, DSA2 Att Setting 0dB)

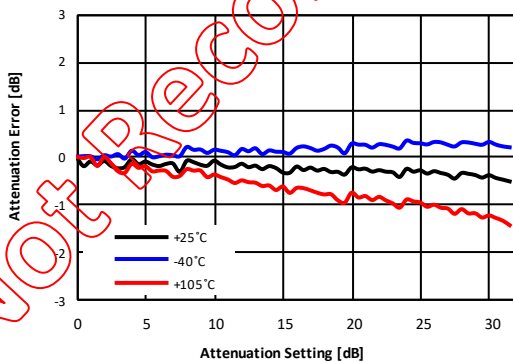
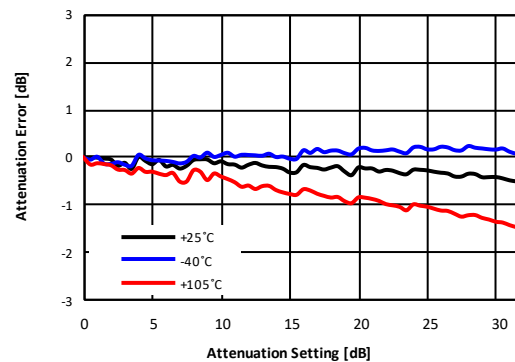


Figure 32. Attenuation Error vs Attenuation Setting over Temperature (@1GHz, DSA2 Control, DSA1 Att Setting 0dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 0.6-1GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 11.

Figure 33. 0.5dB Step Attenuation vs Attenuation Setting
over Major Attenuation Setting(DSA1 Control, DSA2 Att Setting 0dB @+25°C)

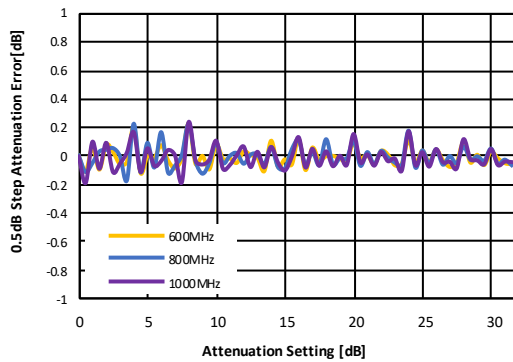
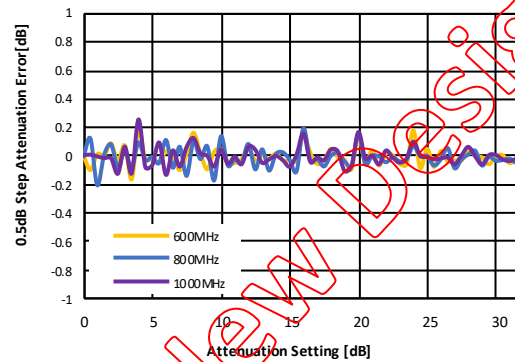


Figure 34. 0.5dB Step Attenuation vs Attenuation Setting
over Major Attenuation Setting(DSA2 Control, DSA1 Att Setting 0dB @+75°C)



Not Recommended for New Designs

DUAL DIGITAL VARIABLE GAIN AMPLIFIER

0.5GHz — 3.8GHz

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 1.7-2.2GHz)

Typical Performance Data @ 25°C and AMP_V_{DD} = 5V, DSA_V_{DD} = 3.3V unless otherwise noted and Application Circuit refer to Table 13.

Table 13. Application Circuit : 1.7 - 2.2GHz

Schematic Diagram		BOM		Remark
Ref	Size	Value		
C3	0402	5.6nH		
C2	0402	4pF		
L2	0402	3.9nH		
C25	0402	22pF		
C22	0402	NC		
C23	0402	22pF		
C24	0402	1uF		
C16	0402	1.2nH		
C15	0402	18 ohm		3dB Pad
C17	0402	300 ohm		
C18	0402	300 ohm		
C14	0402	1.2nH		
C11	0402	5.6nH		
C9	0402	4pF		
C10	0402	NC		
L1	0402	5.6nH		
C37	0402	22pF		
C7	0402	22pF		
C8	0402	1uF		
C20	0402	68pF		LC Filter
L4	0402	100nH		
C19	0402	22pF		LC Filter
C12	0402	22pF		
L3	0402	100nH		
C13	0402	68pF		
R15	0402	0 ohm		
C44	0402	5pF		
R8	0402	0 ohm		
R9	0402	10k ohm		
R10	0402	10k ohm		
R11	0402	0 ohm		
R14	0402	0 ohm		
R13	0402	10k ohm		
R12	0402	10k ohm		
C41	0402	NC		
C42	0402	NC		
C45	0402	NC		

NOTE: C1,C38 is 0ohm or Copper
Any other Ref.Des(Power Supply Block), refer to table 19.

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 1.7-2.2GHz)

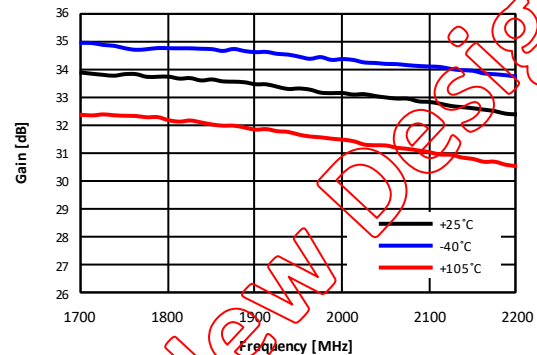
Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13.

Table 14. Typical RF Performance

parameter	Typical Performance			Units
	1.7	1.95	2.2	
Frequency	1.7	1.95	2.2	GHz
Gain ¹	33.9	33.5	32.4	dB
S11	-14.3	-15.8	-11.2	dB
S22	-14.0	-18.7	-24.9	dB
OIP3 ²	38.1	38.2	38.4	dBm
P1dB	21.3	21.2	21.2	dBm
Noise Figure	1.3	1.6	1.8	dB

1. Gain measured with 3dB Attenuation pi Pad between DSA1 and DSA2(Refer to Table13)
 2. OIP3 measured with two tones at an output of 5 dBm per tone separated by 1 MHz.

Figure 35. Gain vs. Frequency over Temperature(DSA1,2 Att setting 0dB)



*Gain measured with 3dB Attenuation pi Pad between DSA1 and DSA2(Refer to Table13)

Figure 36. Gain vs Attenuation Settings over Major Attenuation Setting(DSA1 Att Control, DSA2 Att setting 0dB)

over Major Attenuation Setting(DSA1 Att Control, DSA2 Att setting 0dB)

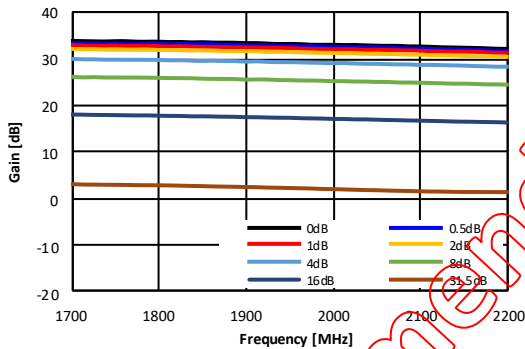


Figure 37. Gain vs Attenuation Settings over Major Attenuation Setting(DSA2 Att Setting 0dB, DSA1 Att Control)

over Major Attenuation Setting(DSA2 Att Setting 0dB, DSA1 Att Control)

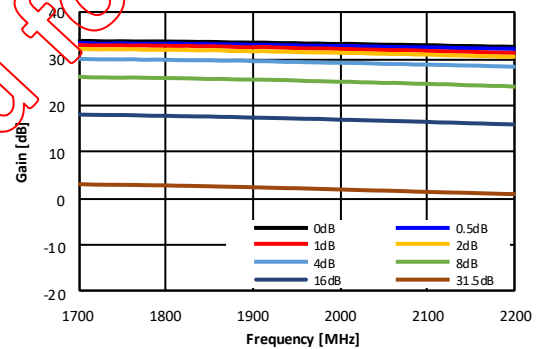
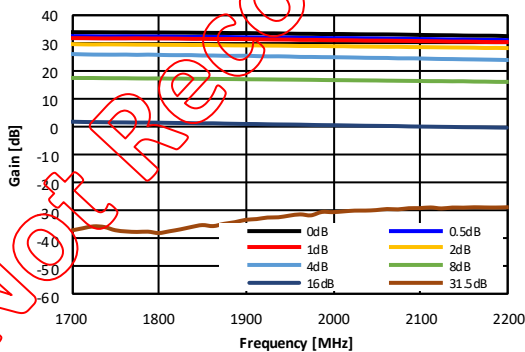


Figure 38. Gain vs Attenuation Settings over Major Attenuation Setting(DSA1, DSA2 DUO Att Control, Attsettingx2)

over Major Attenuation Setting(DSA1, DSA2 DUO Att Control, Attsettingx2)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 1.7-2.2GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13.

Figure 39. Input Return Loss vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)

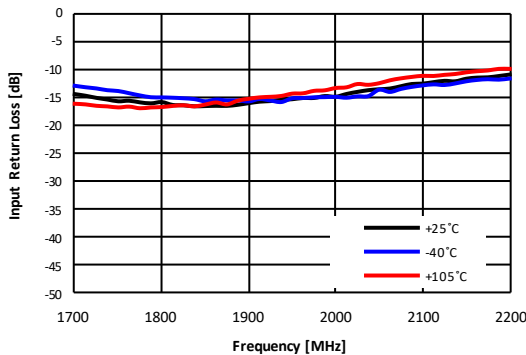


Figure 40. Input Return Loss vs Frequency
over Temperature(DSA1, DSA2 DUO Att Control, Attsetting 31.5dB)

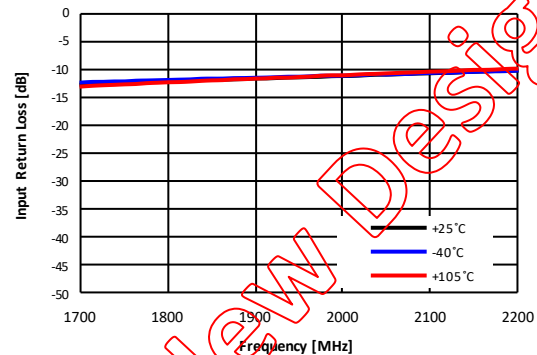


Figure 41. Input Return Loss vs Frequency
over Major Attenuation Setting(DSA1 Att Control, DSA2 Att Setting 0dB)

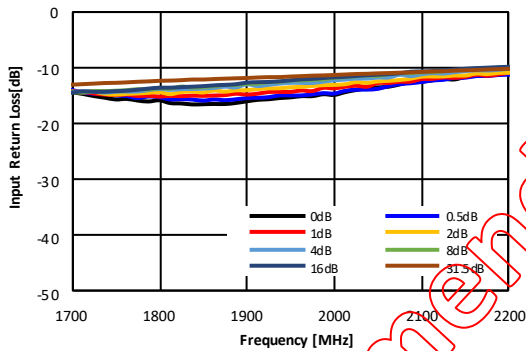


Figure 42. Input Return Loss vs Frequency
over Major Attenuation Setting(DSA2 Att Control, DSA1 Att Setting 0dB)

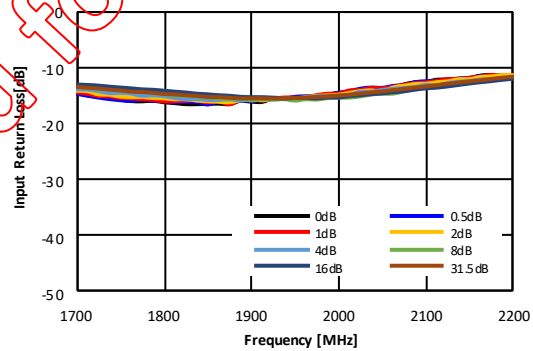


Figure 43. Output Return Loss vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)

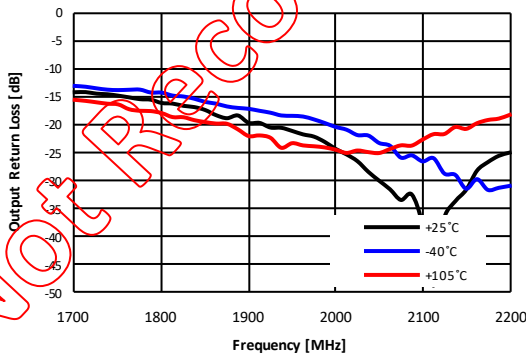
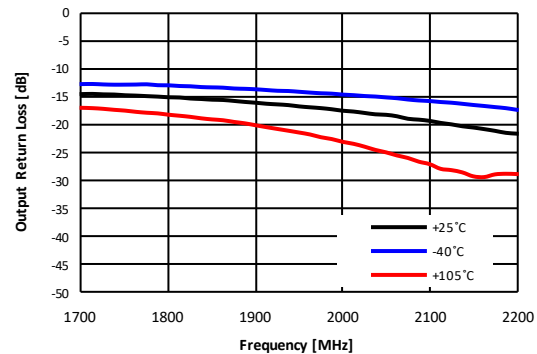


Figure 44. Output Return Loss vs Frequency
over Temperature(DSA1, DSA2 DUO Att Control, Attsetting 31.5dB)



DUAL DIGITAL VARIABLE GAIN AMPLIFIER

0.5GHz — 3.8GHz

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 1.7-2.2GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13.

Figure 45. Output Return Loss vs Frequency
over Major Attenuation Setting(DSA1 Att Control, DSA2 Att Setting 0dB)

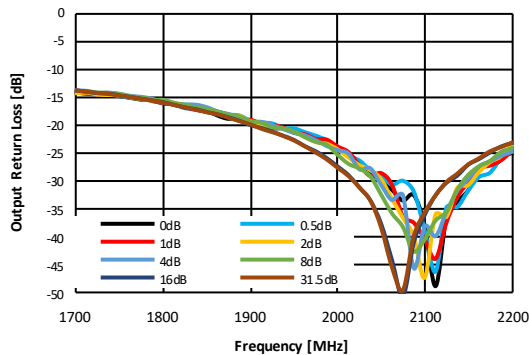


Figure 46. Output Return Loss vs Frequency
over Major Attenuation Setting(DSA1 Att Control, DSA1 Att Setting 0dB)

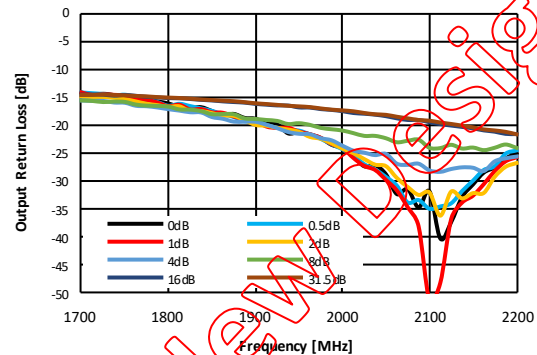


Figure 47. OIP3 vs Output Power
over Temperature(@1.7GHz, DSA1,2 Att Setting 0dB)

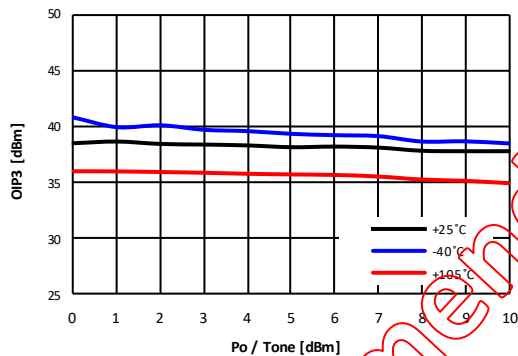


Figure 48. OIP3 vs Output Power
over Temperature(@1.95GHz, DSA1,2 Att Setting 0dB)

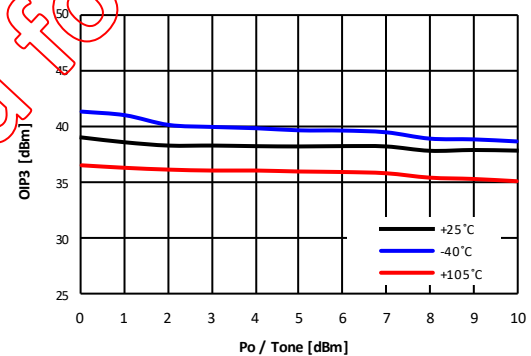


Figure 49. OIP3 vs Output Power
over Temperature(@2.2GHz, DSA1,2 Att Setting 0dB)

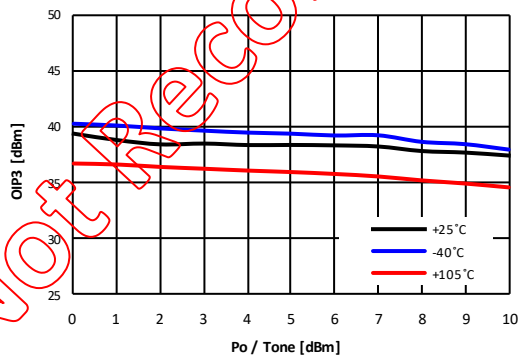
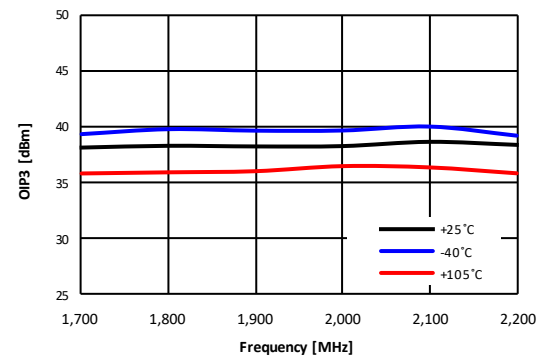


Figure 50. OIP3 vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)



DUAL DIGITAL VARIABLE GAIN AMPLIFIER

0.5GHz — 3.8GHz

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 1.7-2.2GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13.

Figure 51. OP1dB vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)

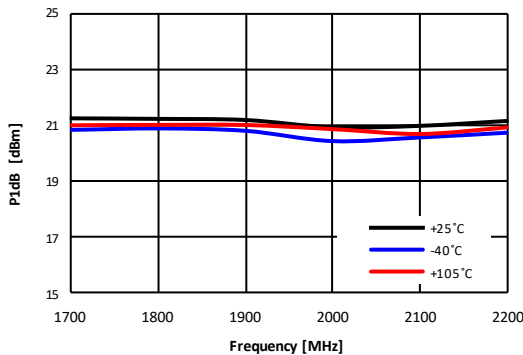


Figure 52. NF vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)

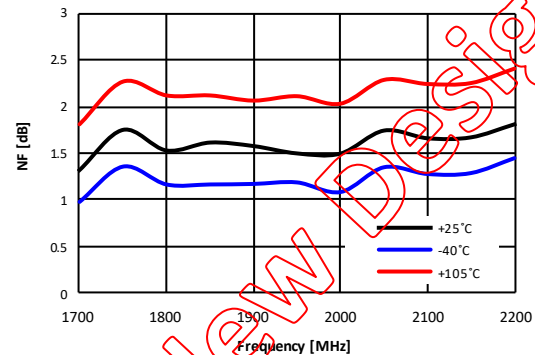


Figure 53. Attenuation Error vs Frequency
over Major Attenuation Setting(DSA1 Control, DSA2 Att Setting 0dB @+25°C)

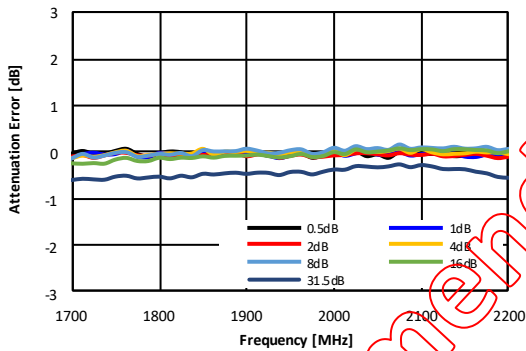


Figure 54. Attenuation Error vs Frequency
over Major Attenuation Setting(DSA2 Control, DSA1 Att Setting 0dB @+25°C)

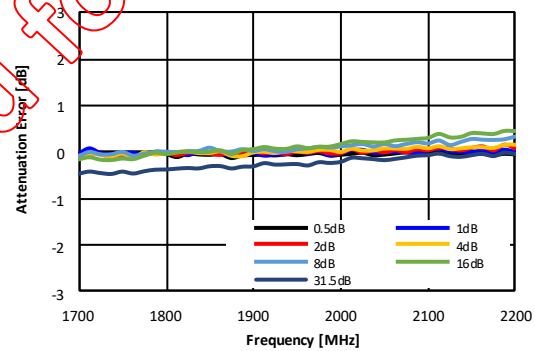


Figure 55. Attenuation Error vs Attenuation Setting
over Major Frequency(DSA1 Control, DSA2 Att Setting 0dB)

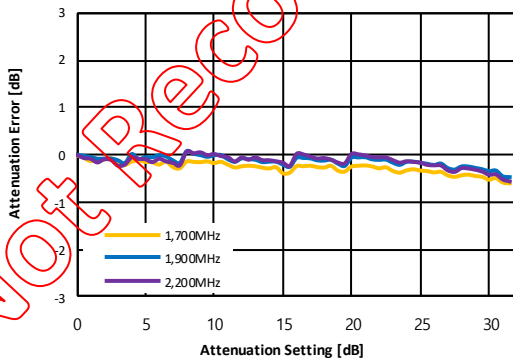
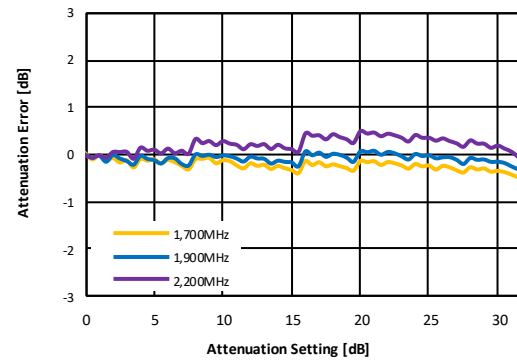


Figure 56. Attenuation Error vs Attenuation Setting
over Major Frequency(DSA2 Control, DSA1 Att Setting 0dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 1.7-2.2GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13.

Figure 57. Attenuation Error vs Attenuation Setting over Temperature (@1.7GHz, DSA1 Control, DSA2 Att Setting 0dB)

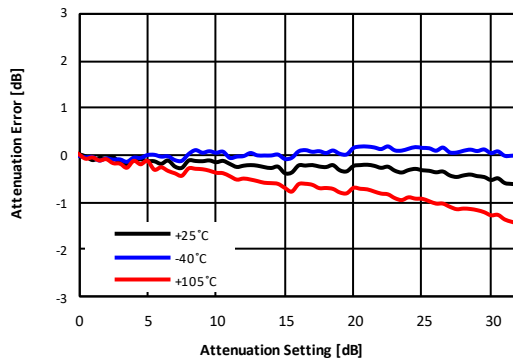


Figure 58. Attenuation Error vs Attenuation Setting over Temperature (@1.7GHz, DSA2 Control, DSA1 Att Setting 0dB)

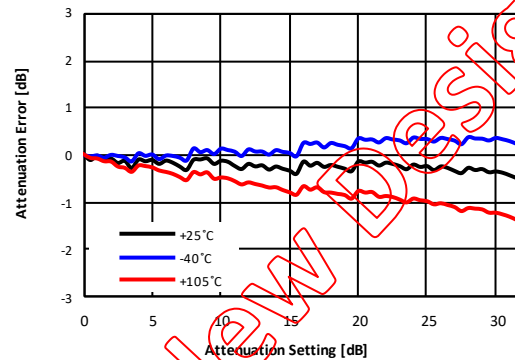


Figure 59. Attenuation Error vs Attenuation Setting over Temperature (@1.95GHz, DSA1 Control, DSA2 Att Setting 0dB)

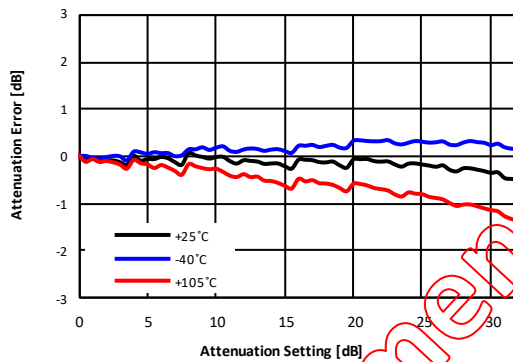


Figure 60. Attenuation Error vs Attenuation Setting over Temperature (@1.95GHz, DSA2 Control, DSA1 Att Setting 0dB)

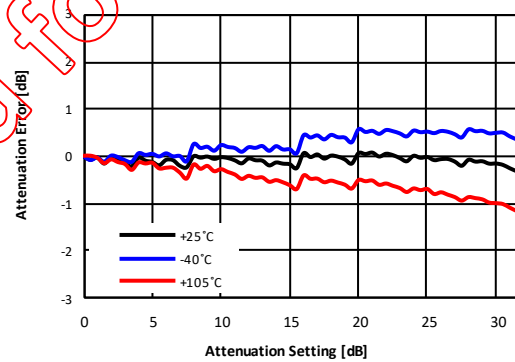


Figure 61. Attenuation Error vs Attenuation Setting over Temperature (@2.2GHz, DSA1 Control, DSA2 Att Setting 0dB)

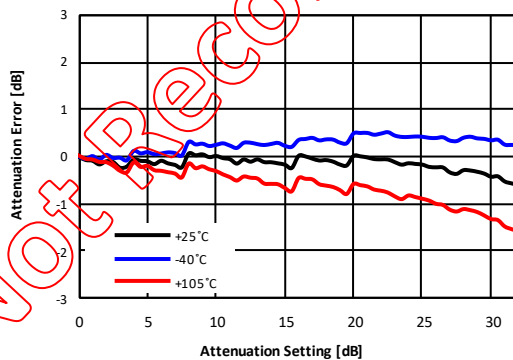
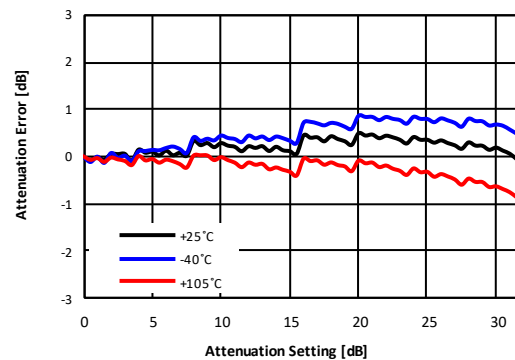


Figure 62. Attenuation Error vs Attenuation Setting over Temperature (@2.2GHz, DSA2 Control, DSA1 Att Setting 0dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 1.7-2.2GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 13.

Figure 63. 0.5dB Step Attenuation vs Attenuation Setting
over Major Attenuation Setting(DSA1 Control, DSA2 Att Setting 0dB @+25°C)

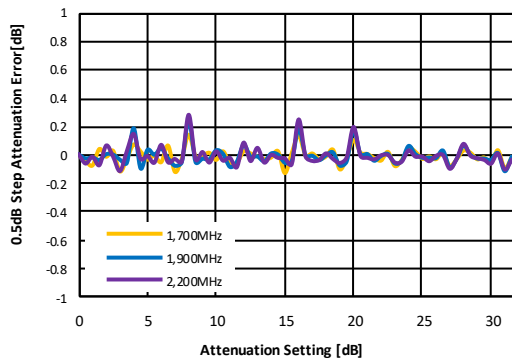
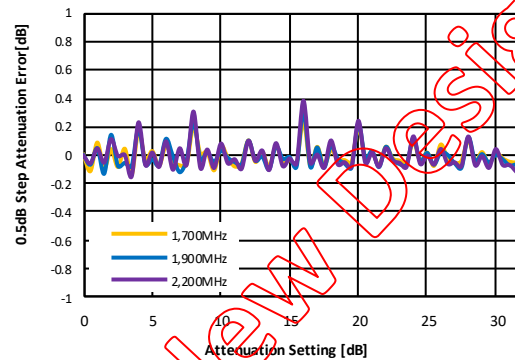


Figure 64. 0.5dB Step Attenuation vs Attenuation Setting
over Major Attenuation Setting(DSA2 Control, DSA1 Att Setting 0dB @+25°C)



Not Recommended for New Designs

DUAL DIGITAL VARIABLE GAIN AMPLIFIER

0.5GHz — 3.8GHz

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 2.3-2.8GHz)

Typical Performance Data @ 25°C and AMP_V_{DD} = 5V, DSA_V_{DD} = 3.3V unless otherwise noted and Application Circuit refer to Table 15.

Table 15. Application Circuit : 2.3 - 2.8GHz

Schematic Diagram		BOM		Remark
Ref	Size	Value		
C3	0402	0.5pF		
C2	0402	22pF		
L2	0402	2.7nH		
C25	0402	22pF		
C22	0402	NC		
C23	0402	22pF		
C24	0402	1uF		
C16	0402	22pF		
C15	0402	12 ohm		2dB Pad
C17	0402	430 ohm		
C18	0402	430 ohm		
C14	0402	22pF		
C11	0402	NC		
C9	0402	22pF		
C10	0402	NC		
L1	0402	3.6nH		
C37	0402	22pF		
C7	0402	22pF		
C8	0402	1uF		
C20	0402	68pF		LC Filter
L4	0402	100nH		
C19	0402	22pF		
C12	0402	22pF		LC Filter
L3	0402	100nH		
C13	0402	68pF		
R15	0402	0 ohm		
C44	0402	NC		
R8	0402	0 ohm		
R9	0402	10k ohm		
R10	0402	10k ohm		
R11	0402	0 ohm		
R14	0402	0 ohm		
R13	0402	10k ohm		
R12	0402	10k ohm		
C41	0402	22pF		
C42	0402	22pF		
C45	0402	1uF		

NOTE: C1, C38 is 0ohm or Copper
Any other Ref.Des(Power Supply Block), refer to table 19.

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 2.3-2.8GHz)

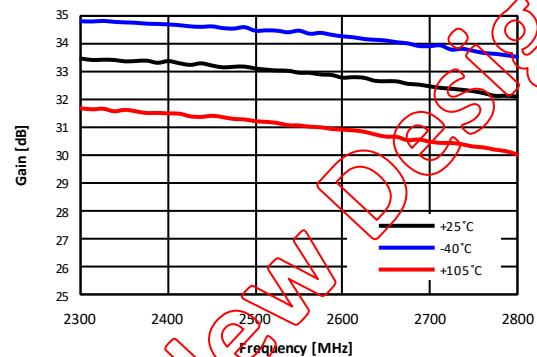
Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15.

Table 16. Typical RF Performance

parameter	Typical Performance			Units
	2.3	2.55	2.8	
Frequency	2.3	2.55	2.8	GHz
Gain ¹	33.5	33.1	32.0	dB
S11	-13.3	-16.9	-17.0	dB
S22	-17.9	-18.7	-15.9	dB
OIP3 ²	38.0	38.2	38.4	dBm
P1dB	20.6	20.8	20.3	dBm
Noise Figure	1.7	1.7	1.8	dB

1. Gain measured with 2dB Attenuation pi Pad between DSA1 and DSA2(Refer to Table15)
 2. OIP3 measured with two tones at an output of 5 dBm per tone separated by 1 MHz.

Figure 65. Gain vs. Frequency over Temperature(DSA1,2 Att setting 0dB)



*Gain measured with 2dB Attenuation pi Pad between DSA1 and DSA2(Refer to Table15)

Figure 66. Gain vs Attenuation Settings over Major Attenuation Setting(DSA1 Att Control, DSA2 Att setting 0dB)

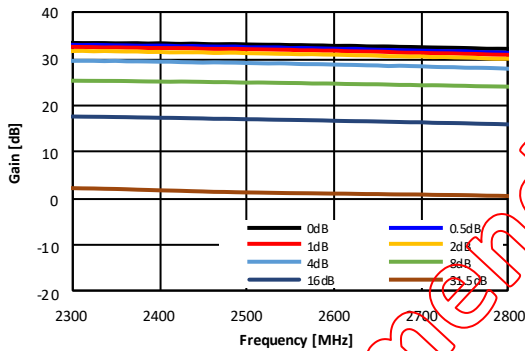


Figure 67. Gain vs Attenuation Settings over Major Attenuation Setting(DSA2 Att Setting 0dB, DSA1 Att Control)

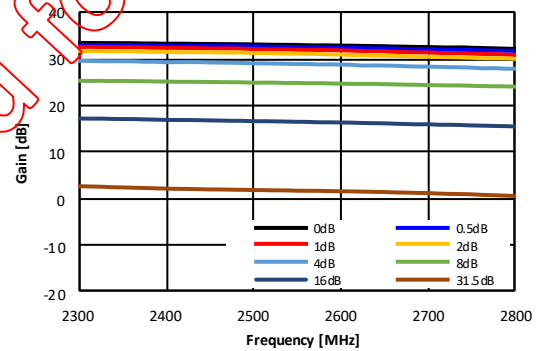
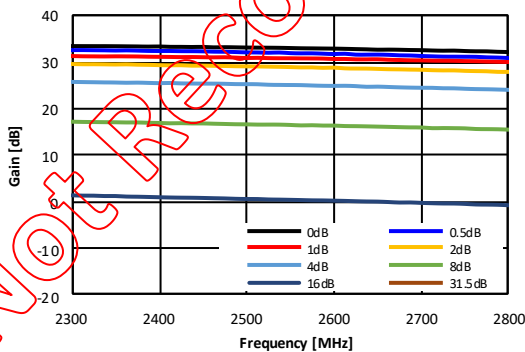


Figure 68. Gain vs Attenuation Settings over Major Attenuation Setting(DSA1, DSA2 DUO Att Control, Attsettingx2 dB)



DUAL DIGITAL VARIABLE GAIN AMPLIFIER

0.5GHz — 3.8GHz

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 2.3-2.8GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15.

Figure 69. Input Return Loss vs Frequency over Temperature(DSA1,2 Att Setting 0dB)

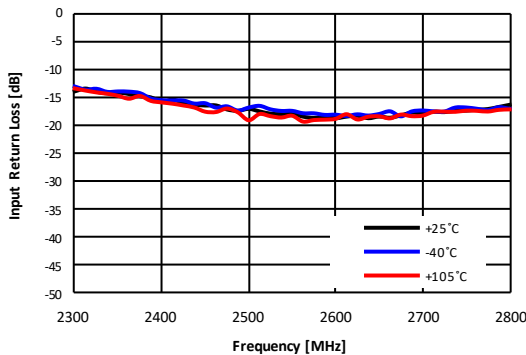
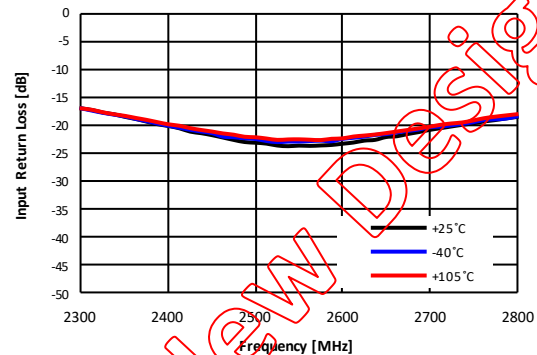


Figure 70. Input Return Loss vs Frequency over Temperature(DSA1, DSA2 DUO Att Control, Attsetting 31.5dB)



*Att setting x2 means a total of 4dB DSA1 2dB and DSA2 2dB, when att setting is 2dB.

Figure 71. Input Return Loss vs Frequency over Major Attenuation Setting(DSA1 Att Control, DSA2 Att Setting 0dB)

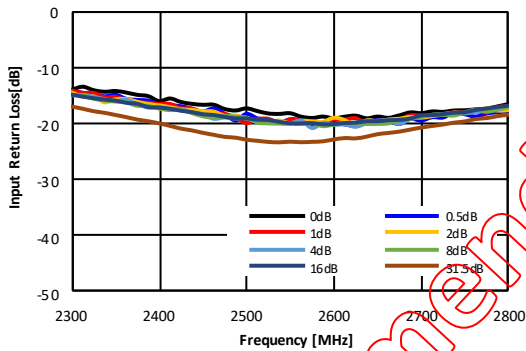


Figure 72. Input Return Loss vs Frequency over Major Attenuation Setting(DSA2 Att Control, DSA1 Att Setting 0dB)

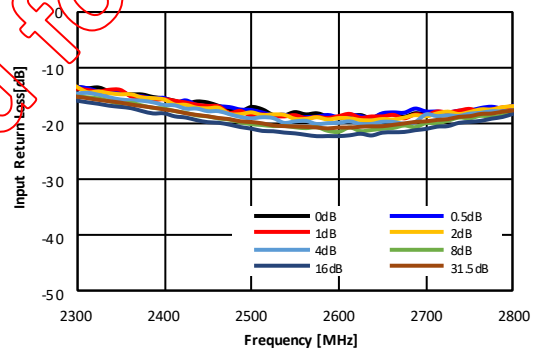


Figure 73. Output Return Loss vs Frequency over Temperature(DSA1,2 Att Setting 0dB)

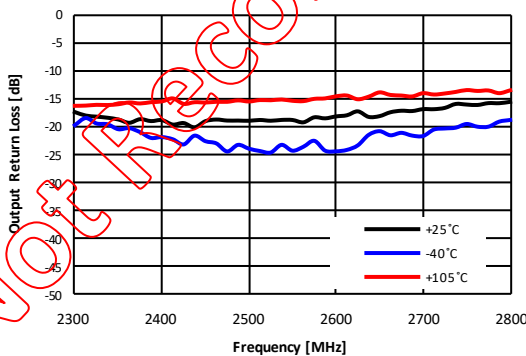
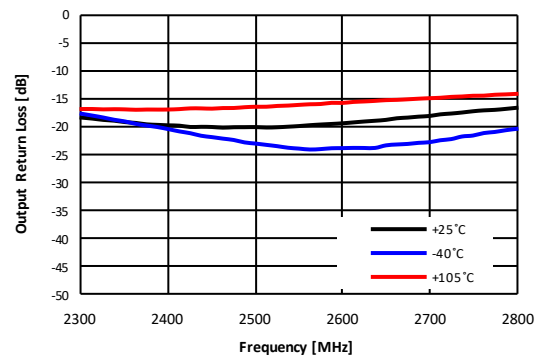


Figure 74. Output Return Loss vs Frequency over Temperature(DSA1, DSA2 DUO Att Control, Attsetting 31.5dB)



DUAL DIGITAL VARIABLE GAIN AMPLIFIER

0.5GHz — 3.8GHz

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 2.3-2.8GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15.

Figure 75. Output Return Loss vs Frequency
over Major Attenuation Setting(DSA1 Att Control, DSA2 Att Setting 0dB)

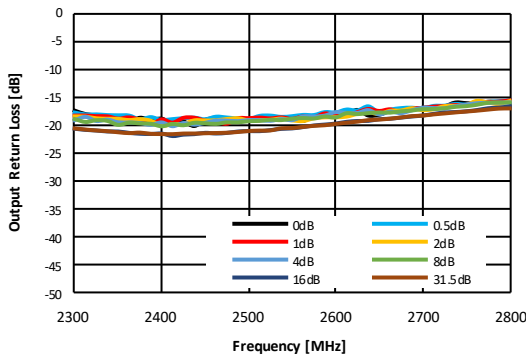


Figure 76. Output Return Loss vs Frequency
over Major Attenuation Setting(DSA2 Att Control, DSA1 Att Setting 0dB)

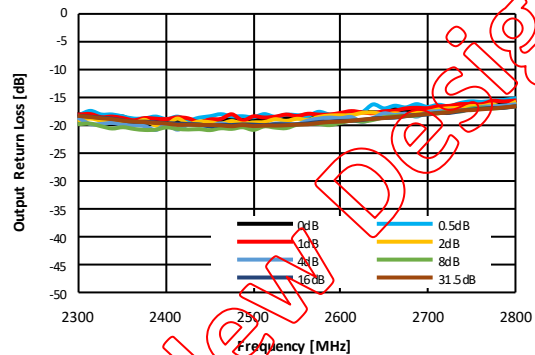


Figure 77. OIP3 vs Output Power
over Temperature(@2.3GHz, DSA1,2 Att Setting 0dB)

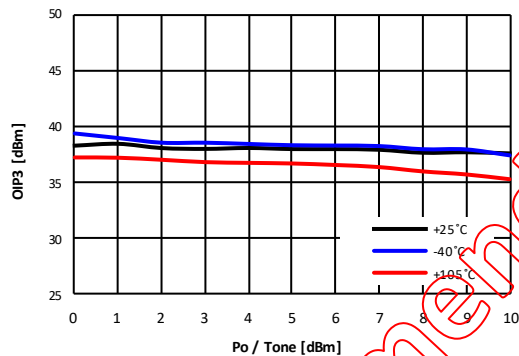


Figure 78. OIP3 vs Output Power
over Temperature(@2.55GHz, DSA1,2 Att Setting 0dB)

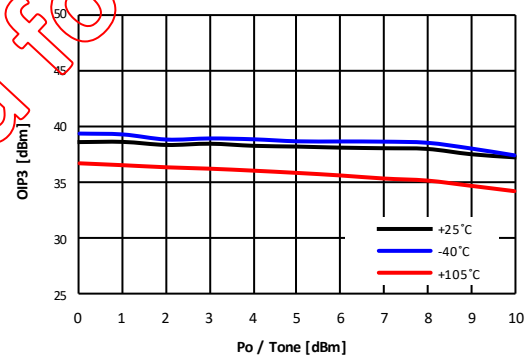


Figure 79. OIP3 vs Output Power
over Temperature(@2.8GHz, DSA1,2 Att Setting 0dB)

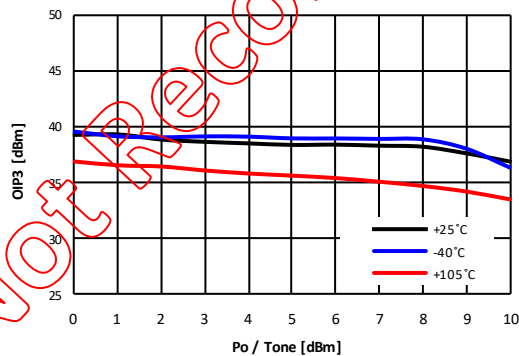
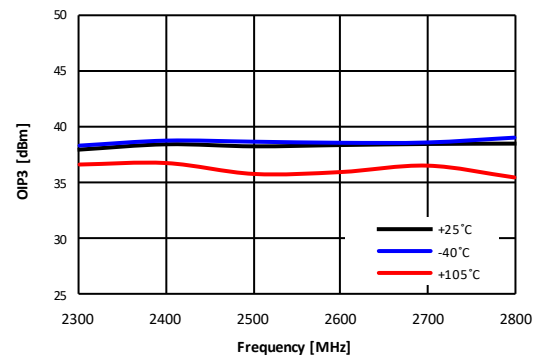


Figure 80. OIP3 vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 2.3-2.8GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15.

Figure 81. OP1dB vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)

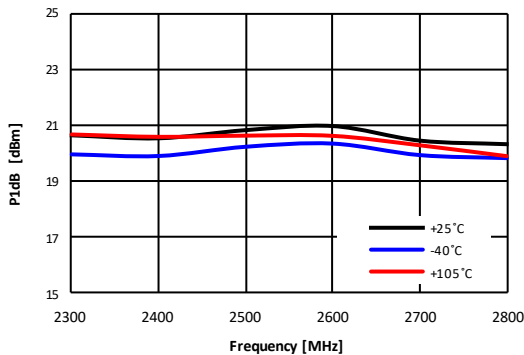


Figure 82. NF vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)

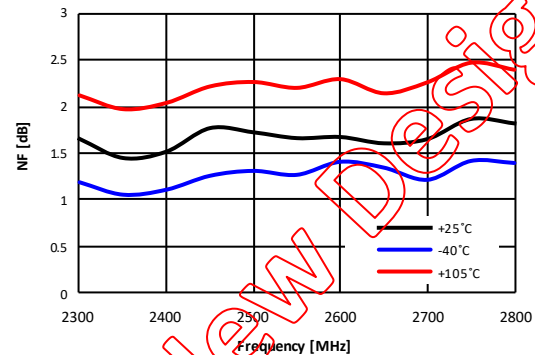


Figure 83. Attenuation Error vs Frequency
over Major Attenuation Setting(DSA1 Control, DSA2 Att Setting 0dB @+25°C)

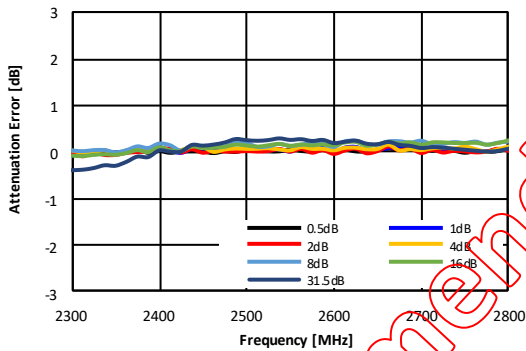


Figure 84. Attenuation Error vs Frequency
over Major Attenuation Setting(DSA2 Control, DSA1 Att Setting 0dB @+25°C)

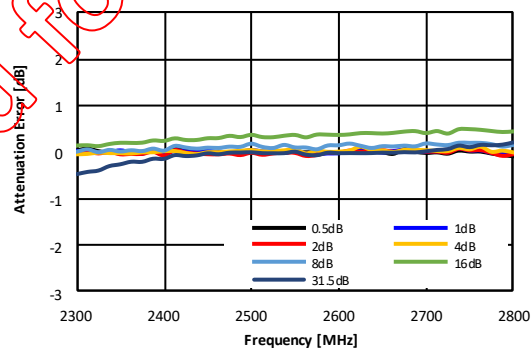


Figure 85. Attenuation Error vs Attenuation Setting
over Major Frequency(DSA1 Control, DSA2 Att Setting 0dB)

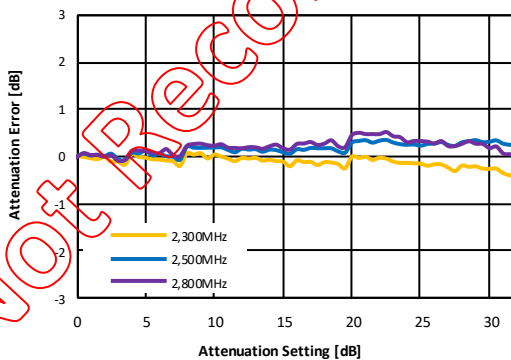
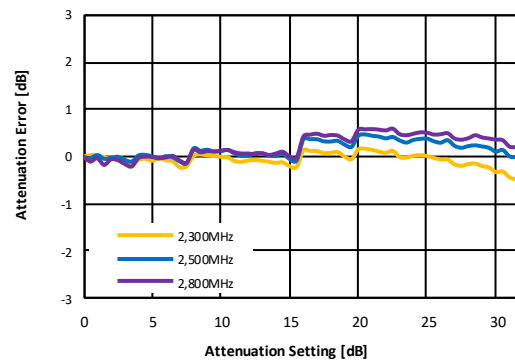


Figure 86. Attenuation Error vs Attenuation Setting
over Major Frequency(DSA2 Control, DSA1 Att Setting 0dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 2.3-2.8GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15.

Figure 87. Attenuation Error vs Attenuation Setting
over Temperature (@2.3GHz, DSA1 Control, DSA2 Att Setting 0dB)

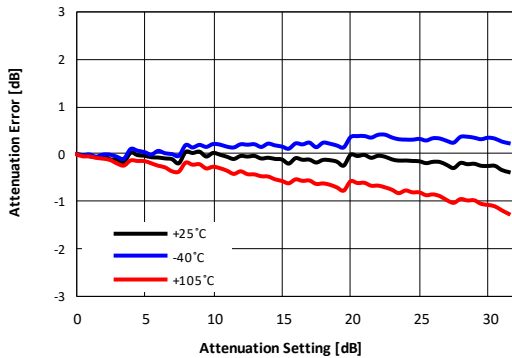


Figure 88. Attenuation Error vs Attenuation Setting
over Temperature (@2.3GHz, DSA2 Control, DSA1 Att Setting 0dB)

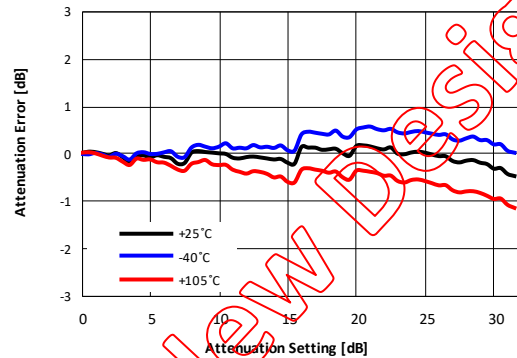


Figure 89. Attenuation Error vs Attenuation Setting
over Temperature (@2.55GHz, DSA1 Control, DSA2 Att Setting 0dB)

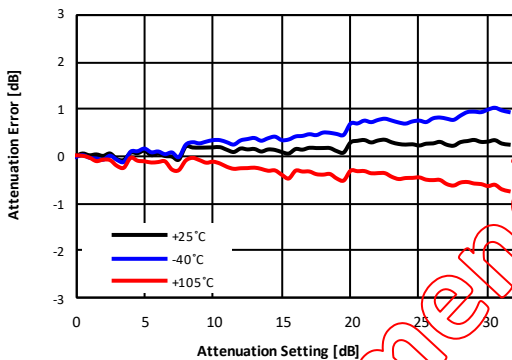


Figure 90. Attenuation Error vs Attenuation Setting
over Temperature (@2.55GHz, DSA2 Control, DSA1 Att Setting 0dB)

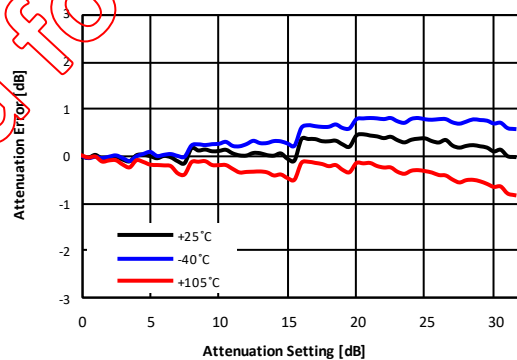


Figure 91. Attenuation Error vs Attenuation Setting
over Temperature (@2.8GHz, DSA1 Control, DSA2 Att Setting 0dB)

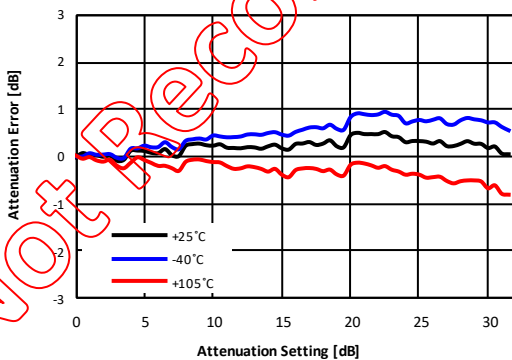
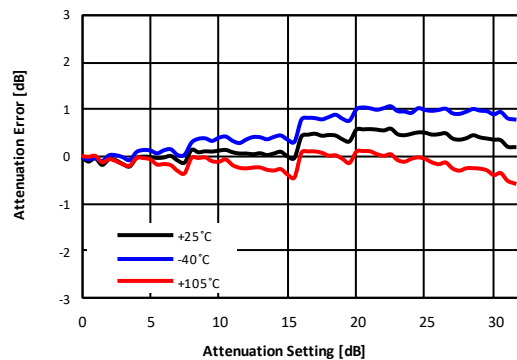


Figure 92. Attenuation Error vs Attenuation Setting
over Temperature (@2.8GHz, DSA2 Control, DSA1 Att Setting 0dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 2.3-2.8GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 15.

Figure 93. 0.5dB Step Attenuation vs Attenuation Setting
over Major Attenuation Setting(DSA1 Control, DSA2 Att Setting 0dB @+25°C)

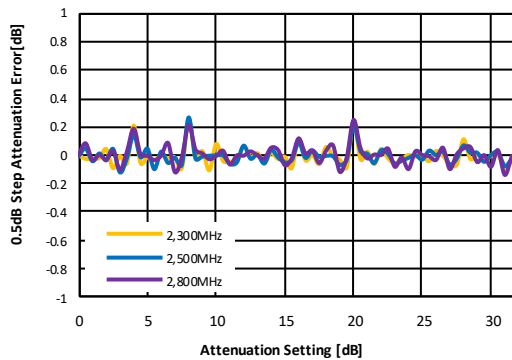
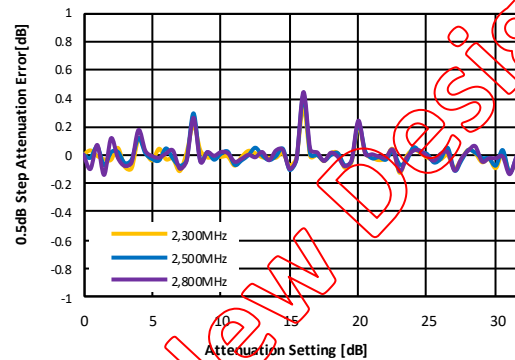


Figure 94. 0.5dB Step Attenuation vs Attenuation Setting
over Major Attenuation Setting(DSA2 Control, DSA1 Att Setting 0dB @+25°C)



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0.5GHz — 3.8GHz

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 3.3-3.8GHz)

Typical Performance Data @ 25°C and AMP_V_{DD} = 5V, DSA_V_{DD} = 3.3V unless otherwise noted and Application Circuit refer to Table 17.

Table 17. Application Circuit : 3.3 - 3.8GHz

Schematic Diagram		BOM		Remark
Ref	Size	Value		
C3	402	0.5pF		
C2	402	2.7pF		
L2	402	2nH		
C25	402	22pF		
C22	402	NC		
C23	402	22pF		
C24	402	1uF		
C16	402	22pF		
C15	402	0 ohm		
C17	402	NC		
C18	402	22pF		
C14	402	22pF		
C11	402	0.5pF		
C9	402	10pF		
C10	402	NC		
L1	402	2nH		
C37	402	10pF		
C7	402	22pF		
C8	402	1uF		
C20	402	68pF		LC Filter
L4	402	100nH		LC Filter
C19	402	22pF		
C12	402	22pF		LC Filter
L3	402	100nH		LC Filter
C13	402	68pF		
R15	402	0 ohm		
C44	402	NC		
R8	402	0 ohm		
R9	402	10k ohm		
R10	402	10k ohm		
R11	402	0 ohm		
R14	402	0 ohm		
R13	402	10k ohm		
R12	402	10k ohm		
C41	402	22pF		
C42	402	22pF		
C45	402	1uF		
C5	402	0.5pF		
C40	402	0.5pF		

NOTE: C1,C38 is 0ohm or Copper
Any other Ref.Des(Power Supply Block), refer to table 19.

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 3.3-3.8GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17.

Table 18. Typical RF Performance

parameter	Typical Performance			Units
	3.3	3.5	3.8	
Frequency				GHz
Gain	32	30.8	30.2	dB
S11	-15.3	-21.3	-29.3	dB
S22	-10.0	-7.7	-6.5	dB
OIP3 ¹	37.5	38.7	39.2	dBm
P1dB	19.2	18.9	18.4	dBm
Noise Figure	2.0	2.2	2.4	dB

1. OIP3 measured with two tones at an output of 5 dBm per tone separated by 1 MHz.

Figure 95. Gain vs. Frequency over Temperature (DSA1,2 Att setting 0dB)

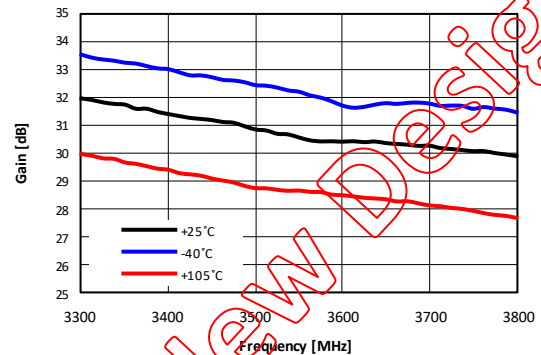


Figure 96. Gain vs Attenuation Settings over Major Attenuation Setting (DSA1 Att Control, DSA2 Att setting 0dB)

over Major Attenuation Setting (DSA1 Att Control, DSA2 Att setting 0dB)

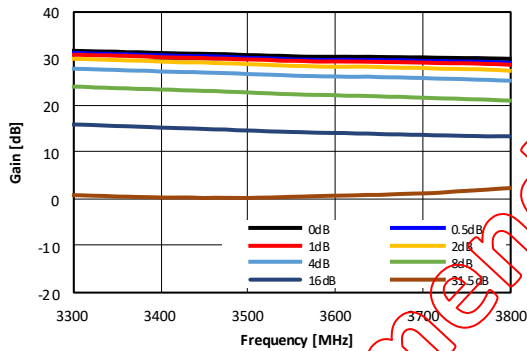


Figure 97. Gain vs Attenuation Settings over Major Attenuation Setting (DSA2 Att Setting 0dB, DSA1 Att Control)

over Major Attenuation Setting (DSA2 Att Setting 0dB, DSA1 Att Control)

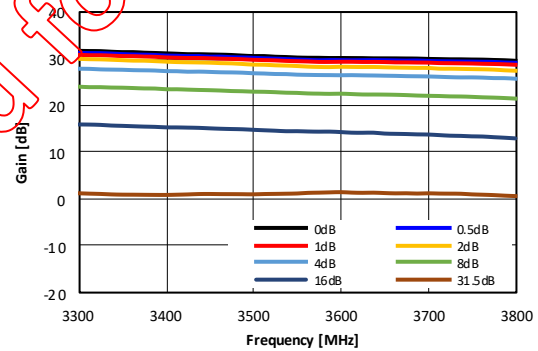
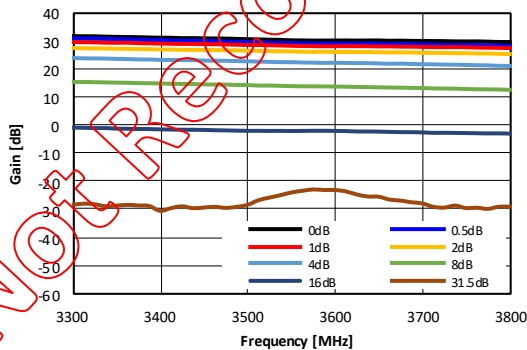


Figure 98. Gain vs Attenuation Settings over Major Attenuation Setting (DSA1, DSA2 DUO Att Control, Attsettingx2 dB)

over Major Attenuation Setting (DSA1, DSA2 DUO Att Control, Attsettingx2 dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 3.3-3.8GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17.

Figure 99. Input Return Loss vs Frequency over Temperature (DSA1,2 Att Setting 0dB)

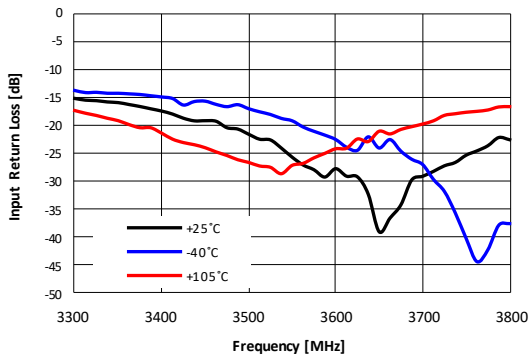
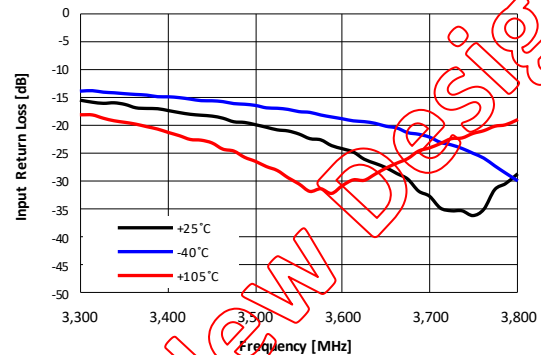


Figure 100. Input Return Loss vs Frequency over Temperature (DSA1, DSA2 DUO Att Control, Attsetting 31.5dB)



*Att setting x2 means a total of 4dB DSA1 2dB and DSA2 2dB, when att setting is 2dB.

Figure 101. Input Return Loss vs Frequency over Major Attenuation Setting (DSA1 Att Control, DSA2 Att Setting 0dB)

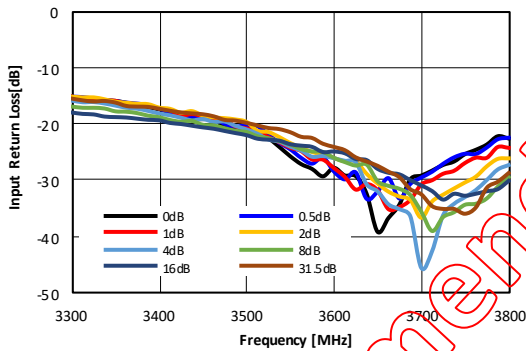


Figure 102. Input Return Loss vs Frequency over Major Attenuation Setting (DSA2 Att Control, DSA1 Att Setting 0dB)

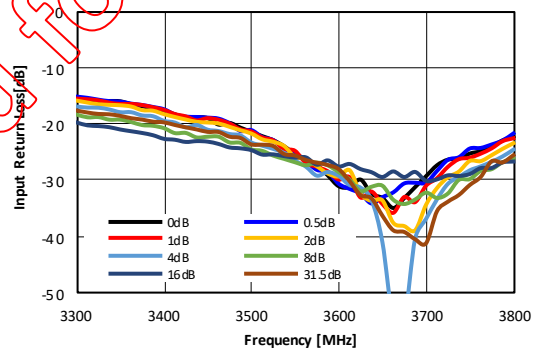


Figure 103. Output Return Loss vs Frequency over Temperature (DSA1,2 Att Setting 0dB)

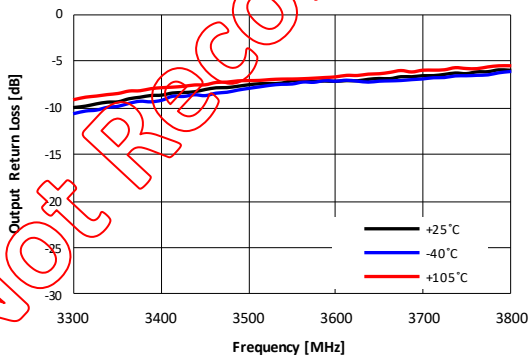
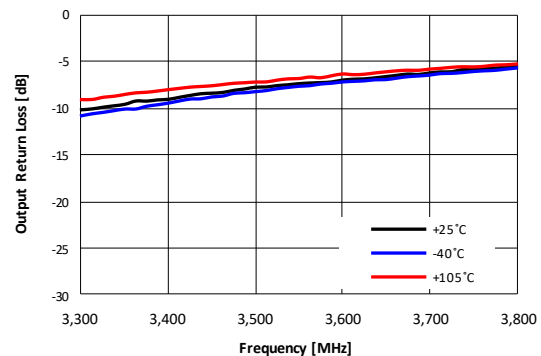


Figure 104. Output Return Loss vs Frequency over Temperature (DSA1, DSA2 DUO Att Control, Attsetting 31.5dB)



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0.5GHz — 3.8GHz

Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 3.3-3.8GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17.

Figure 105. Output Return Loss vs Frequency
over Major Attenuation Setting(DSA1 Att Control, DSA2 Att Setting 0dB)

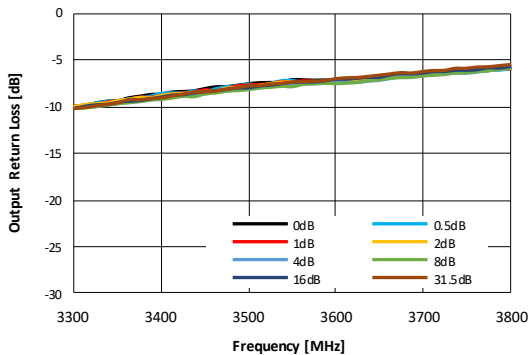


Figure 106. Output Return Loss vs Frequency
over Major Attenuation Setting(DSA2 Att Control, DSA1 Att Setting 0dB)

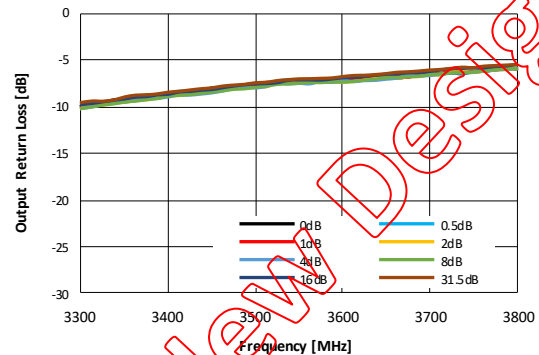


Figure 107. OIP3 vs Output Power
over Temperature(@3.3GHz, DSA1,2 Att Setting 0dB)

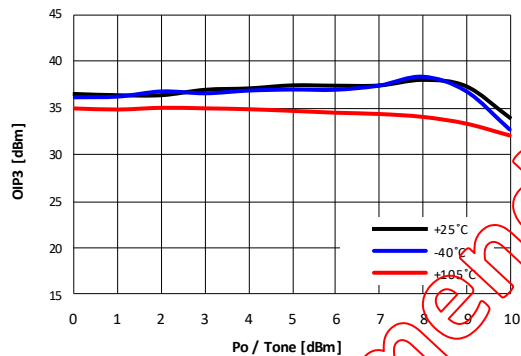


Figure 108. OIP3 vs Output Power
over Temperature(@3.5GHz, DSA1,2 Att Setting 0dB)

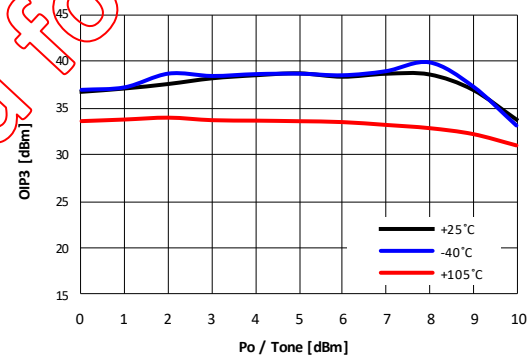


Figure 109. OIP3 vs Output Power
over Temperature(@3.8GHz, DSA1,2 Att Setting 0dB)

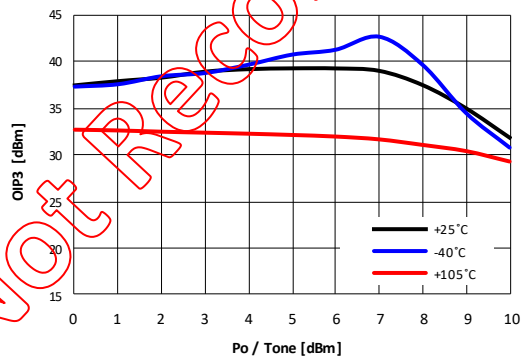
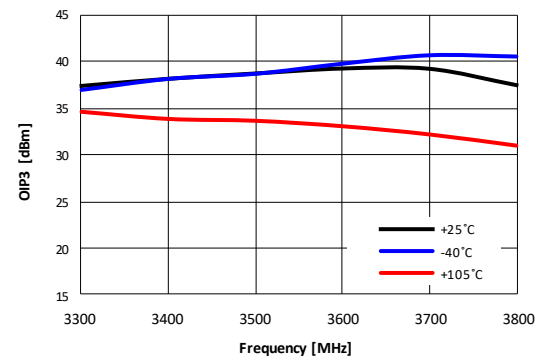


Figure 110. OIP3 vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 3.3-3.8GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17.

Figure 111. OP1dB vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)

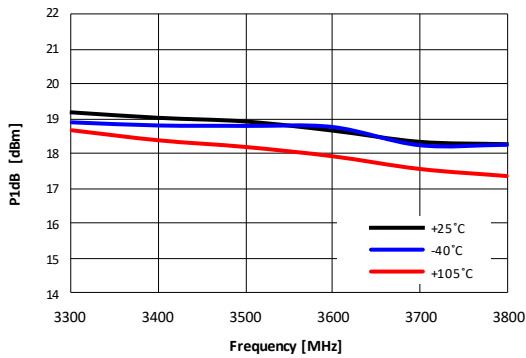


Figure 112. NF vs Frequency
over Temperature(DSA1,2 Att Setting 0dB)

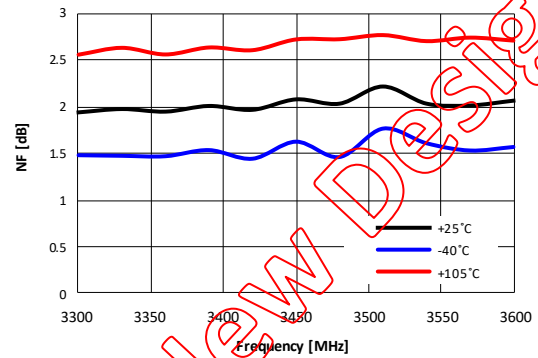


Figure 113. Attenuation Error vs Frequency
over Major Attenuation Setting(DSA1 Control, DSA2 Att Setting 0dB @+25°C)

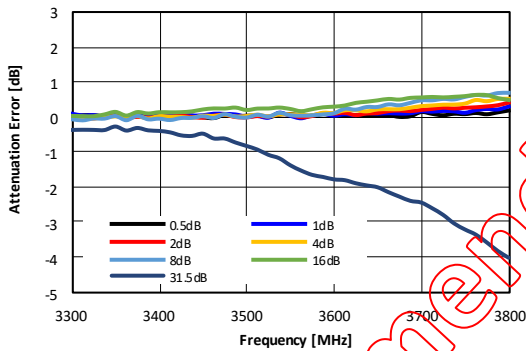


Figure 114. Attenuation Error vs Frequency
over Major Attenuation Setting(DSA2 Control, DSA1 Att Setting 0dB @+25°C)

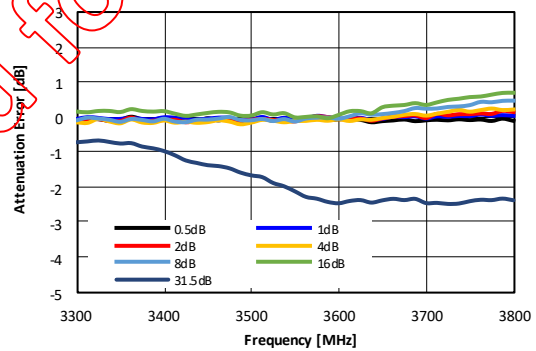


Figure 115. Attenuation Error vs Attenuation Setting
over Major Frequency(DSA1 Control, DSA2 Att Setting 0dB)

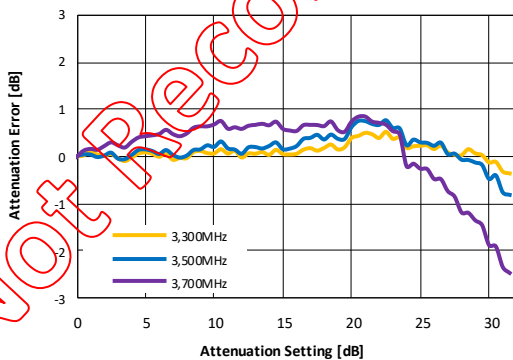
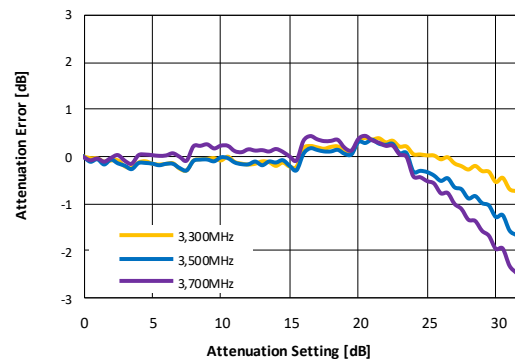


Figure 116. Attenuation Error vs Attenuation Setting
over Major Frequency(DSA2 Control, DSA1 Att Setting 0dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 3.3-3.8GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17.

Figure 117. Attenuation Error vs Attenuation Setting over Temperature (@3.3GHz, DSA1 Control, DSA2 Att Setting 0dB)

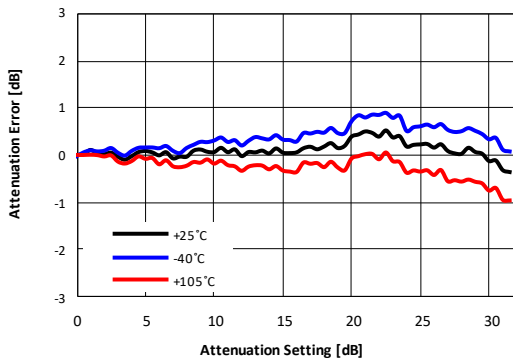


Figure 118. Attenuation Error vs Attenuation Setting over Temperature (@3.3GHz, DSA2 Control, DSA1 Att Setting 0dB)

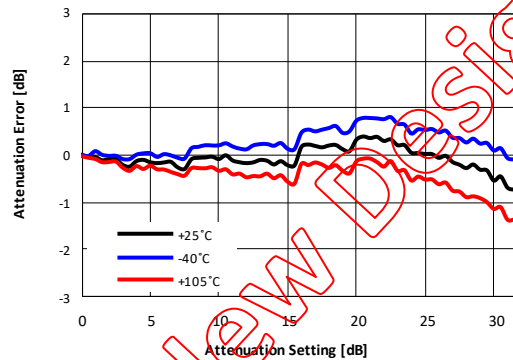


Figure 119. Attenuation Error vs Attenuation Setting over Temperature (@3.5GHz, DSA1 Control, DSA2 Att Setting 0dB)

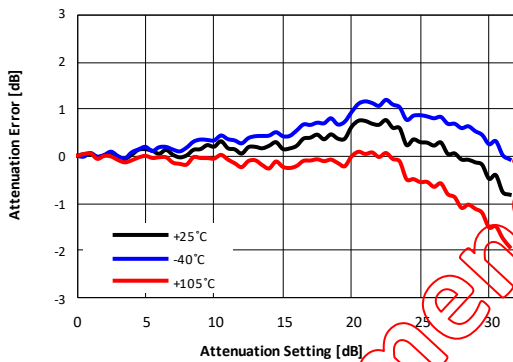


Figure 120. Attenuation Error vs Attenuation Setting over Temperature (@3.5GHz, DSA2 Control, DSA1 Att Setting 0dB)

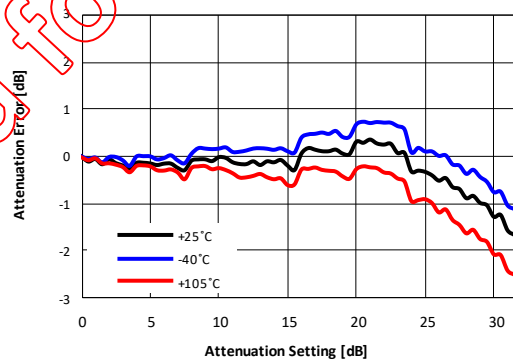


Figure 121. Attenuation Error vs Attenuation Setting over Temperature (@3.8GHz, DSA1 Control, DSA2 Att Setting 0dB)

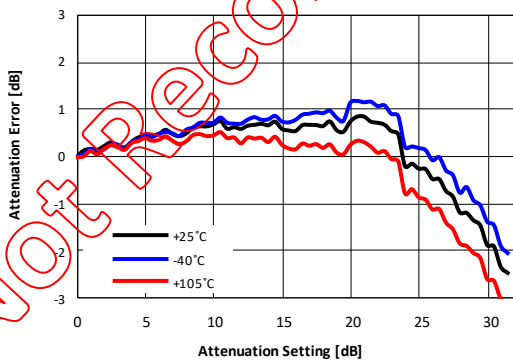
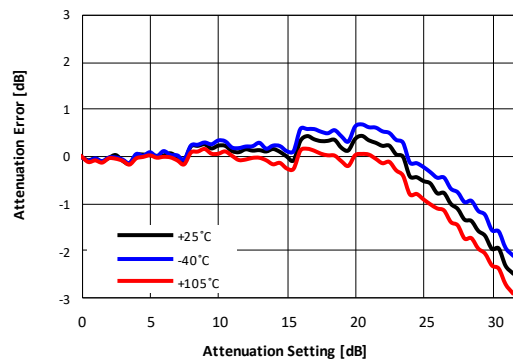
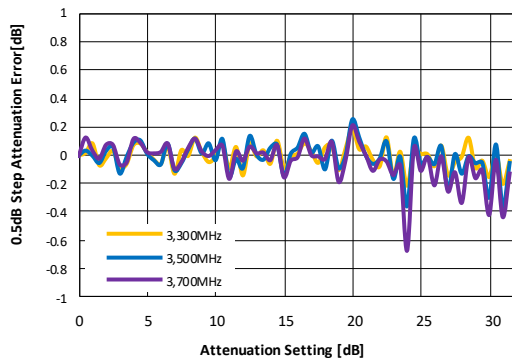
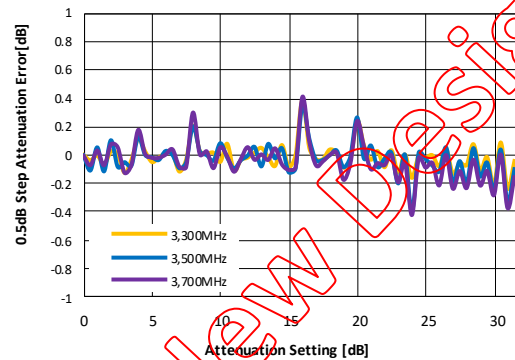


Figure 122. Attenuation Error vs Attenuation Setting over Temperature (@3.8GHz, DSA2 Control, DSA1 Att Setting 0dB)



Typical RF Performance Plot - BVA2182 EVK - PCB (Application Circuit: 3.3-3.8GHz)

Typical Performance Data @ 25°C and AMP_VDD = 5V, DSA_VDD = 3.3V unless otherwise noted and Application Circuit refer to Table 17.

Figure 123. 0.5dB Step Attenuation vs Attenuation Setting
 over Major Attenuation Setting(DSA1 Control, DSA2 Att Setting 0dB @+25°C)

Figure 124. 0.5dB Step Attenuation vs Attenuation Setting
 over Major Attenuation Setting(DSA2 Control, DSA1 Att Setting 0dB @+25°C)


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0.5GHz — 3.8GHz

Figure 125. Evaluation Board Schematic

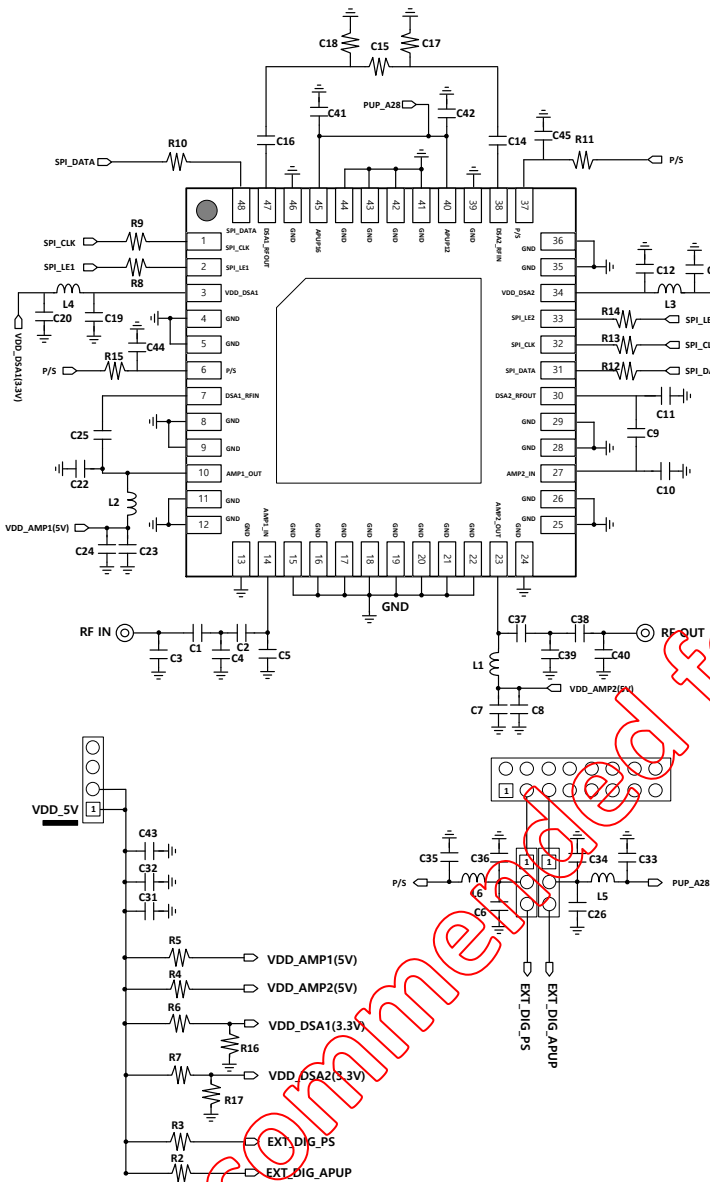


Table 19. Power Supply Block BOM

No	BOM			Remark
	Ref	Size	Value	
1	C43	0402	10uF	Tantal
2	C32	0402	4.7uF	
3	C31	0402	NC	
4	R5	0402	0ohm	
5	R4	0402	0ohm	
6	R6	0402	5.6k ohm	
7	R16	0402	91 k ohm	
8	R7	0402	5.6k ohm	
9	R17	0402	91k ohm	
10	R3	0402	NC	
11	R2	0402	NC	
12	C36	0402	68pF	
13	L6	0402	100nH	
14	C35	0402	22pF	
15	C6	0402	NC	
16	C33	0402	22pF	
17	C5	0402	100nH	
18	C34	0402	68pF	
19	C26	0402	NC	
20	C27	0402	100pF	
21	C28	0402	100pF	
22	C29	0402	100pF	
23	C30	0402	100pF	

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Figure 126. Evaluation Board PCB Layer Information

EM825B Er: 4.6~4.8	<p>COPPER :1oz + 0.5oz (plating), Top Layer</p> <p>P.P : (0.2+0.06+0.06) TOTAL = 0.32mm</p> <p>COPPER :1oz (GND), Inner Layer</p>	<p>FINISH THICKNESS :1.55T</p>
MTC Er:4.6	<p>CORE : 0.73mm</p> <p>COPPER :1oz, Inner Layer</p>	
EM825B Er:4.6~4.8	<p>P.P : (0.2+0.06+0.06) TOTAL = 0.32mm</p> <p>COPPER :1oz + 0.5oz (plating), Bottom Layer</p>	

Figure 127. Evaluation Board Layout

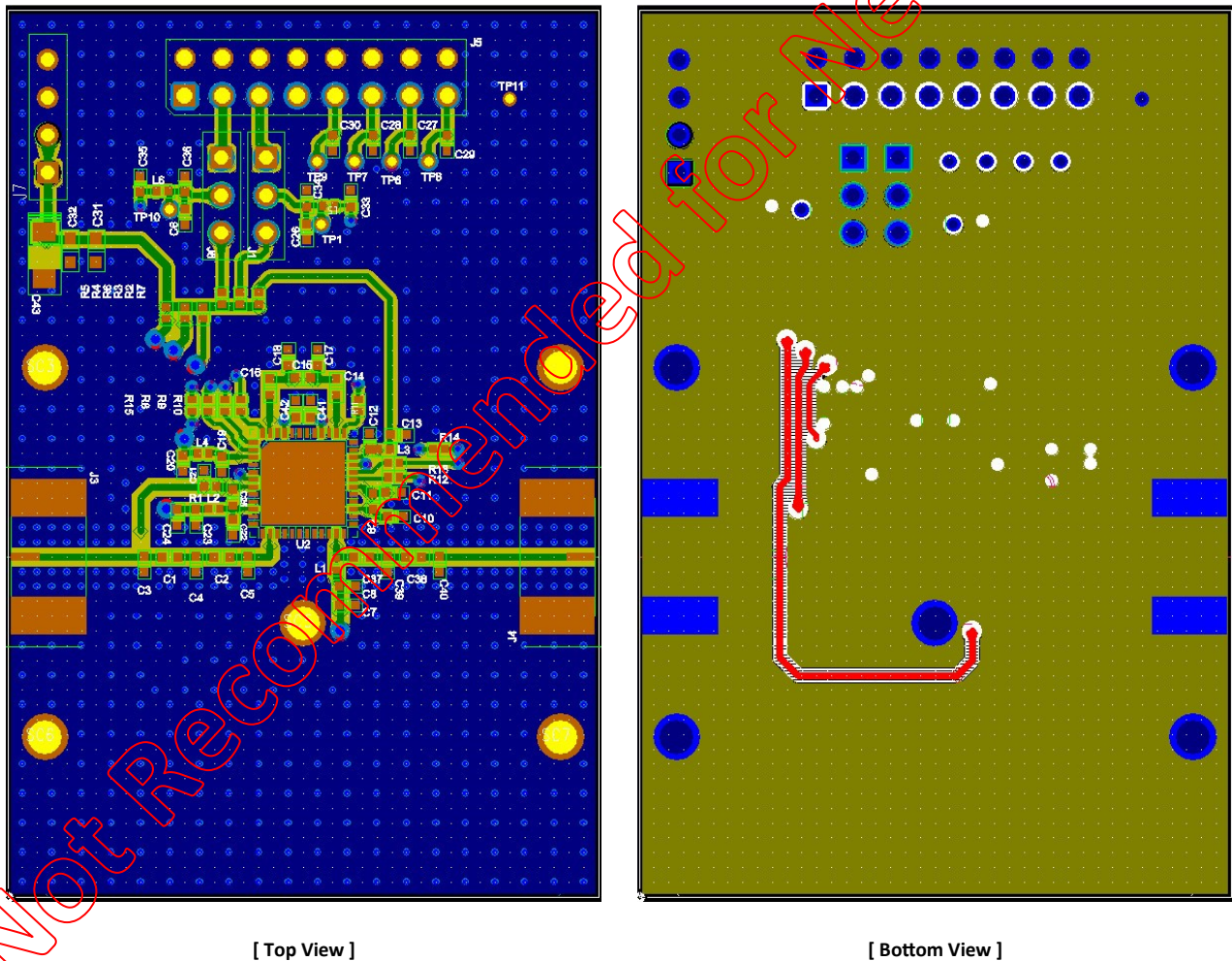
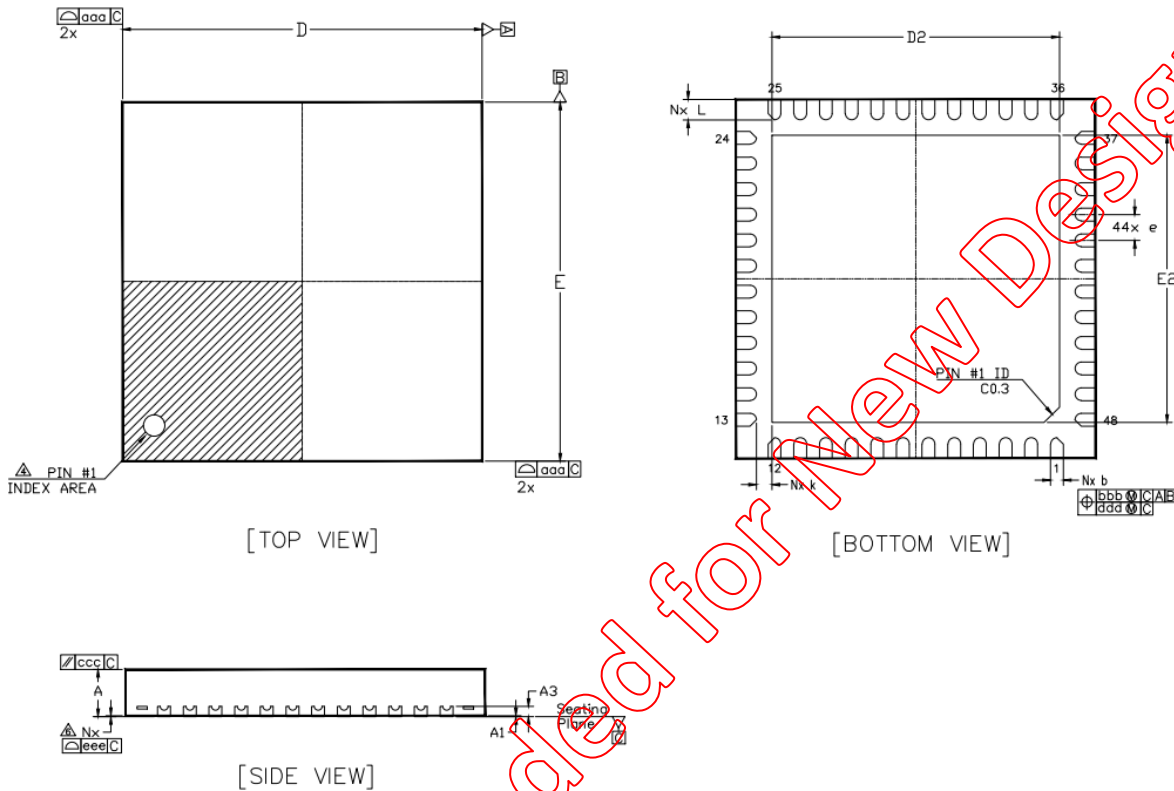


Figure 128. Packing outline Dimension

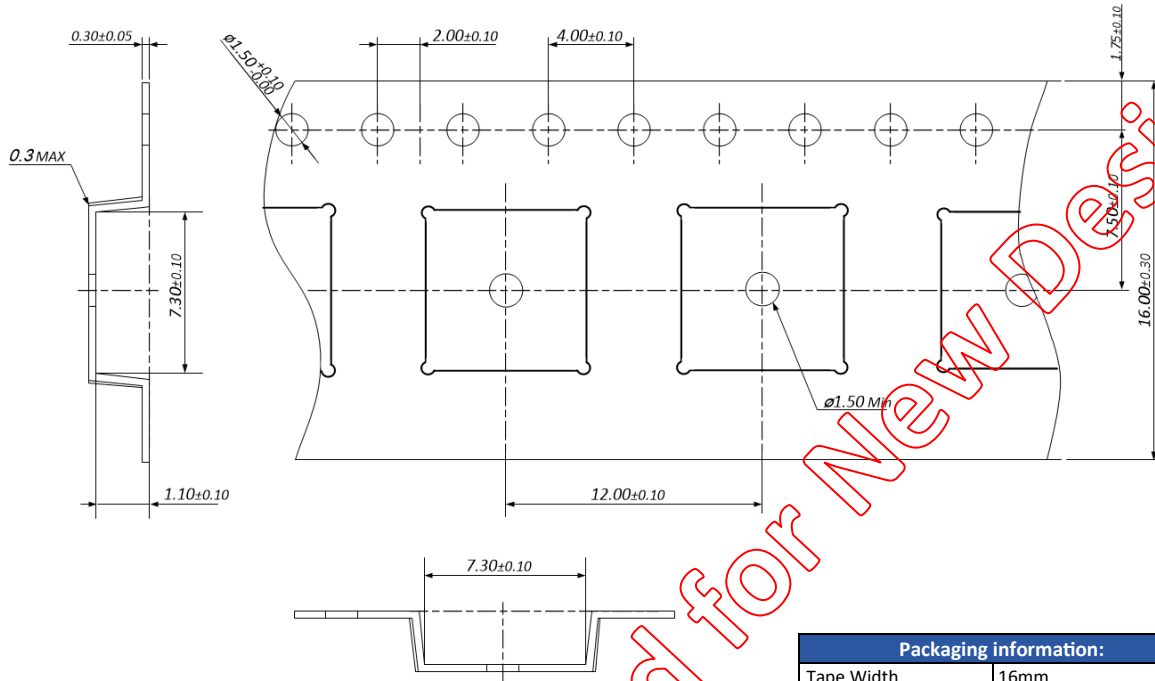


NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5–2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals each D and E side respectively.
6. Coplanarity applies to the terminals and all other bottom surface metallization.

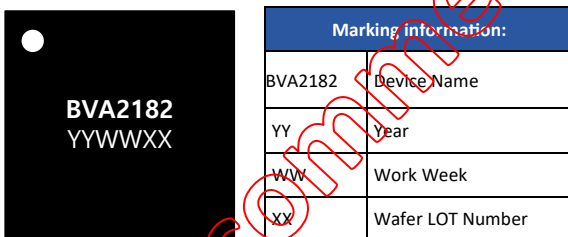
Dimension Table (Notes 1,2)					
Symbol	Thickness	Min	Nominal	Max	Note
A		0.80	0.90	1.00	
A1		0.00	0.02	0.05	
A3		---	0.203 Ref.	---	
b		0.20	0.25	0.30	
D		6.90	7.00	7.10	
E		6.90	7.00	7.10	
e		0.50 BSC			
D2		5.50	5.60	5.70	
E2		5.50	5.60	5.70	
K		0.2	---	---	
L		0.35	0.40	0.45	
aaa		0.15			
bbb		0.10			
ccc		0.10			
ddd		0.05			
eee		0.08			
N		48		3	
ND		12		5	
NE		12		5	

Figure 130. Tape & Reel



Packaging information:	
Tape Width	16mm
Reel Size	7 inches
Device Cavity Pitch	12mm
Devices Per Reel	1,000EA

Figure 131. Package Marking



Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	Class 1C
Value:	±1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JS-001-2017
MSL Rating:	Level 1 at +260°C convection reflow
Standard:	JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

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