BVA3144C

Medium Power Digital Variable Gain Amplifier 4400MHz – 5000MHz

Device Features

- Integrated Amp1 + DSA + Amp2 + Amp3
- A Single +5.0V supply
- 4400 - 5000MHz Frequency Range
- 37.3dB Gain @ 4.6GHz
- 4.2dB Noise Figure at max gain setting @ 4.6GHz
- 26.5dBm Output P1dB @ 4.6GHz
- 40dBm Output IP3 @ 4.6GHz
- ACP at 4.6GHz, 50dBc
  - 5GNR 100MBW (±100MHz offset) ≥ 14.5dBm
  - LTE 20MBW(±20MHz offset) ≥ 16.0dBm
- Attenuation : 0.25 dB step up to 31.75 dB
- Glitch-less attenuation state transitions
- High attenuation accuracy
  ±(0.3 + 5% x ATT) @ 4.4 - 5.0GHz
- Programming Interface
  - Serial / Parallel (Bypass Mode)
- Lead-free/RoHS2-compliant 28-lead 6mm x 6mm x 1.07mm SIP LGA SMT Package

28-lead 6mm x 6mm x 1.07mm SIP LGA

Figure 1. Package Type

Product Description

The BVA3144C is a digitally controlled variable gain amplifier (DVGA) in a 6mm x 6mm SIP LGA package, with a frequency range of 4400 to 5000 MHz and an operating VDD of 5.0V.

BVA3144C is high performance and high dynamic range makes it ideally suited for use in 5G/LTE wireless infrastructure and other high performance wireless RF applications.

The BVA3144C is an integration of a high performance digital 7bit step attenuator (DSA) that provides a 31.75 dB attenuation range in 0.25 dB steps, and high linearity broadband gain block amplifiers featuring high ACP and P1dB.

The BVA3144C digital control interface supports serial programming of the attenuator, and includes the reference gain (max gain, bypass) state on the Parallel programing .

The BVA3144C is integrated of two gain blocks (AMP1, AMP2), a digital step attenuator (DSA) and high linearity amplifier (AMP3).

Implementation requires only a few external components, such as matching capacitors on the Input and Output pins. (Don't need DC Blocking Capacitor)

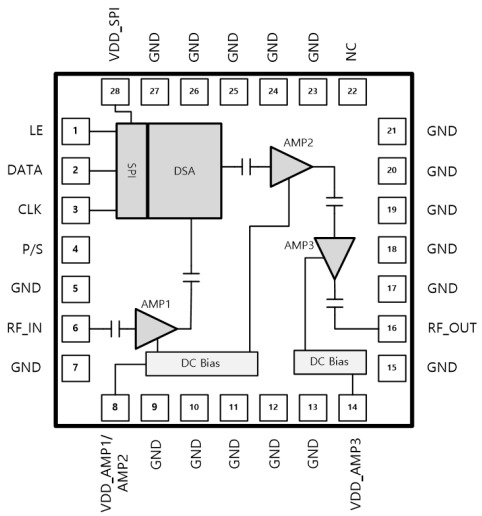


Figure 2. Functional Block Diagram

Application

- 5G/4G/3G wireless Infrastructure
- Small Cells
- Repeaters

Table 1. Electrical Specifications[1]

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			4400		5000	MHz
Gain[2]		ATT = 0dB @ 4.4GHz		37.2		dB
		ATT = 0dB @ 4.6GHz		37.3		
		ATT = 0dB @ 4.8GHz		36.7		
		ATT = 0dB @ 5GHz		35.6		
Attenuation Control range		0.25dB Step		0 - 31.75		dB
Attenuation Step				0.25		dB
Attenuation Accuracy		Any bit or bit combination			±(0.3 + 5% of ATT setting)	dB
Return Loss	Input Return Loss	ATT = 0dB		13.0		dB
	Output Return Loss			14.8		
Output Power for 1dB Compression		ATT = 0dB @ 4.4GHz		26.9		dBm
		ATT = 0dB @ 4.6GHz		26.5		
		ATT = 0dB @ 4.8GHz		26.6		
		ATT = 0dB @ 5GHz		25.7		
Output Third Order Intercept Point[3]		ATT = 0dB @ 4.4GHz		40.0		dBm
		ATT = 0dB @ 4.6GHz		40.0		
		ATT = 0dB @ 4.8GHz		38.0		
		ATT = 0dB @ 5GHz		37.5		
Noise Figure		ATT = 0dB @ 4.4GHz		4.2		dB
		ATT = 0dB @ 4.6GHz		4.2		
		ATT = 0dB @ 4.8GHz		4.5		
		ATT = 0dB @ 5GHz		4.7		
Switching time		50% CTRL to 90% or 10% RF		275		ns
Impedance				50		Ω

1. Device performance : measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+5.0V.
2. Gain data has PCB & Connectors insertion loss de-embedded.
3. OIP3 measured with two tones at an output of 5dBm per tone separated by 1MHz.

Table 2. Typical RF Performance[1]

Parameter	Frequency				Unit
Frequency	**4400**	**4600**	**4800**	**5000**	**MHz**
Gain[2]	37.2	37.3	36.7	35.6	dB
S11	-8.1	-11.3	-14.4	-18.5	dB
S22	-14.1	-14.2	-15.1	-16.1	dB
OIP3[3]	40.0	40.0	38.0	37.5	dBm
P1dB	26.9	26.5	26.6	25.7	dBm
LTE 20M ACP[4]	62.8	62.9	63.0	62.4	dBc
5GNR 100M ACP[5]	56.0	54.5	54.1	54.1	dBc
Noise Figure	4.2	4.2	4.5	4.7	dB

1. Device performance : measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+5.0V.
2. Gain data has PCB & Connectors insertion loss de-embedded.
3. OIP3 measured with two tones at an output of +5 dBm per tone separated by 1 MHz.
4. LTE set-up : 3GPP LTE, E-TM3.1, 20MHz BW, ±20MHz offset, PAR 9.6 at 0.01% Prob. Output power 7dBm. Applied the Noise correlation function of Instrument.
5. 5GNR set-up : 3GPP 5GNR, 100MHz BW, ±100MHz offset. Output Power 7dBm. Applied the Noise correlation function of Instrument.

Table 3. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage	AMP1, DSA, AMP2, AMP3	-0.3		5.5	V
Supply Current	AMP1, DSA, AMP2, AMP3			580	mA
Digital Input voltage	DSA Control Pin (LE, DATA, CLK, P/S)	-0.3		3.6	V
Maximum Input power	AMP1, DSA, AMP2, AMP3			20	dBm
Storage Temperature		-55		+150	℃
Junction Temperature				+150	℃

Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	AMP1+DSA+AMP2+AMP3	4.4		5	GHz
Supply Voltage (VDD)	DSA	3.3	5	5.5	V
	AMP	4.85	5	5.15	V
Supply Current	AMP1+DSA+AMP2+AMP3	270	310	350	mA
DSA control Voltage	Digital input high	1.17		3.6	V
	Digital input low	-0.3		0.63	V
Operating Temperature	AMP1+DSA+AMP2+AMP3	-40		+125	℃

Specifications are not guaranteed over all recommended operating conditions.

Table 5. Package Thermal Characteristics

Parameter	Symbol	Value	Unit
Junction to Case Thermal Resistance	θ_{JC}	21.77	°C/W

Figure 3. Pin Configuration (Top View)

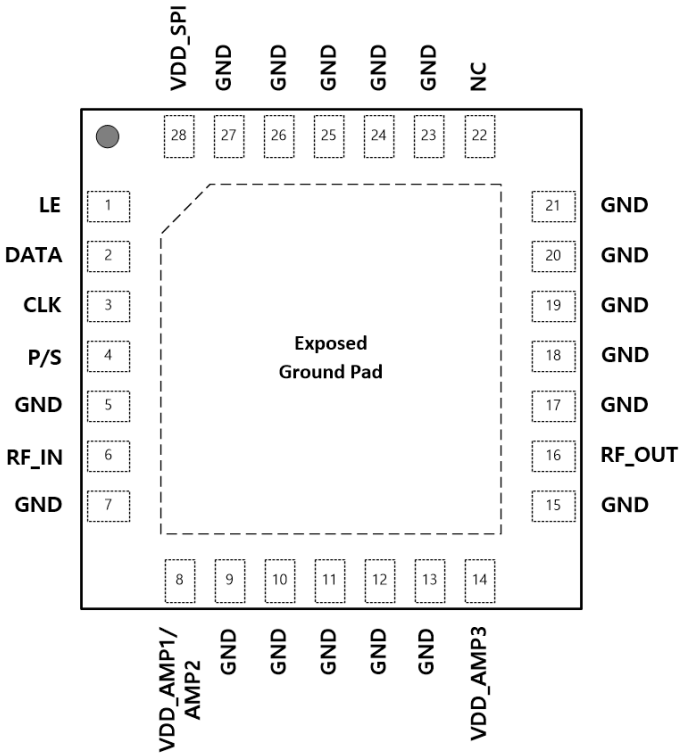


Table 6. Pin Description

Pin	Pin name	Description
1	LE[1]	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial Data Input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial Clock Input.
4	P/S	The P/S bit provides this selection, P/S=Low selecting the Parallel Interface which is the Max. Gain state (Bypass Mode, ATT=0dB) and either P/S=High selecting or floating for the Serial Interface.
6	RF IN	RF Input, matched to 50 ohm. Internally DC blocked.
8	VDD_AMP1/AMP2	Supply Voltage to AMP1 and AMP2. This pin is connected internally to bypass capacitors followed by inductor inside the module.
14	VDD_AMP3	Supply Voltage to AMP3. This pin is connected internally to bypass capacitors followed by inductor inside the module.
16	RF OUT	RF output, matched to 50 ohm. Internally DC blocked.
22	N/C	No connect or open. This pin is not connected.
28	VDD_SPI	SPI and DSA DC supply. This pin is connected to bypass capacitor internally.
5, 7, 9-13, 15 17-21,23-27	GND	RF/DC Ground

1. LE must be Pulled-up to 1.17V - 3.6V to use the Bypass Mode when P/S = Low (Bypass mode, ATT=0dB)

Programming mode

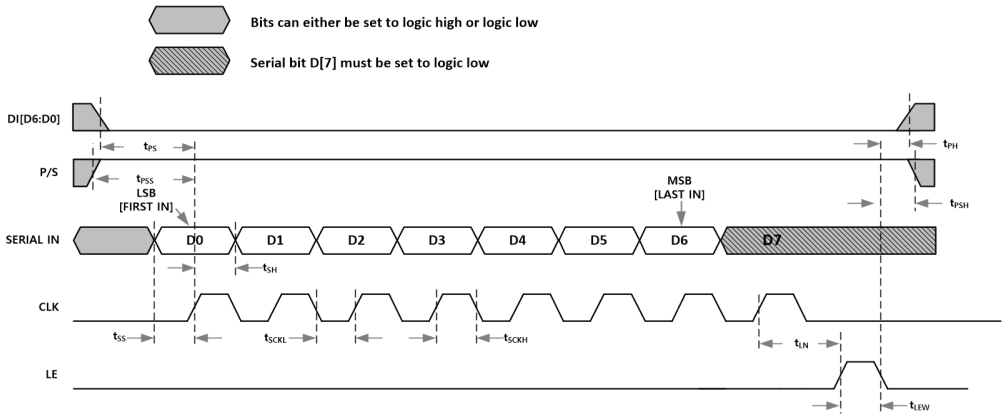
Serial / Parallel (Bypass) Selection

Either a Serial or Parallel interface can be used to control the P/S Pin. The P/S bit provides the selection, with P/S = HIGH or floating selecting the Serial interface and P/S = LOW selecting the Parallel interface (Bypass Mode, Max Gain State).

Table 7. Truth Table for Serial Control Word

Digital Control Input								Attenuation state (dB)
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.25
0	0	0	0	0	0	1	0	0.5
0	0	0	0	0	1	0	0	1.0
0	0	0	0	1	0	0	0	2.0
0	0	0	1	0	0	0	0	4.0
0	0	1	0	0	0	0	0	8.0
0	1	0	0	0	0	0	0	16.0
0	1	1	1	1	1	1	1	31.75

Figure 4. Serial Mode Timing Diagram



Serial Interface

The Serial interface is an 8-bit Serial-In, Parallel-Out shift register buffered by a transparent latch. The 8-bits make up the Attenuation Word that controls the DSA. Figure 4 illustrates an example timing diagram for programming a state.

The Serial interface is controlled using three CMOS compatible signals: SI, Clock (CLK) and LE. The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The Attenuation Word truth table is listed in Table 7. The timing for this operation is defined by Figure 4 (Serial Interface Timing Diagram) and Table 8 (Serial Interface Timing Specifications).

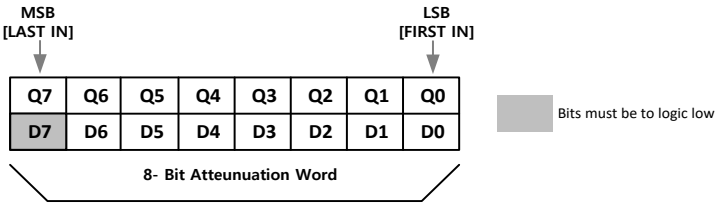
Table 8. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{CLK}	Serial data clock frequency			10	MHz
t_{PS}	Parallel data setup time	100			ns
t_{PH}	Parallel data hold time	100			ns
t_{PSS}	Parallel/Serial setup time	100			ns
t_{PSH}	Parallel/Serial hold time	100			ns
t_{SS}	Serial Data setup time	10			ns
t_{SH}	Serial Data hold time	10			ns
t_{SCKH}	Serial clock high time	30			ns
t_{SCKL}	Serial clock low time	30			ns
t_{LN}	LE setup time	10			ns
t_{LEW}	Minimum LE pulse width	30			ns

Serial Register Map

The BVA3144C can be programmed via the serial control on the rising edge of Latch Enable (LE) which loads the last 8-bits data word in the SHIFT Register. Serial Data is clocked in LSB(D0) first.

Figure 5. Serial Register Map



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four, then convert to binary.
For example, to program the 15.75dB state :

4 x 15.75 = 63
D0 - D7 : 00111111

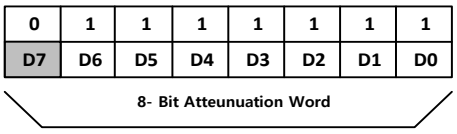
Serial Input : 00111111

0	0	1	1	1	1	1	1
D7	D6	D5	D4	D3	D2	D1	D0

Power-up Control Settings

The BVA3144C will always initialize to the maximum attenuation setting (Atten=31.75dB) on power-up for the Serial mode and will remain in this setting until the user latches in the next programming word.

Figure 6. Default Attenuation word for Power-up state

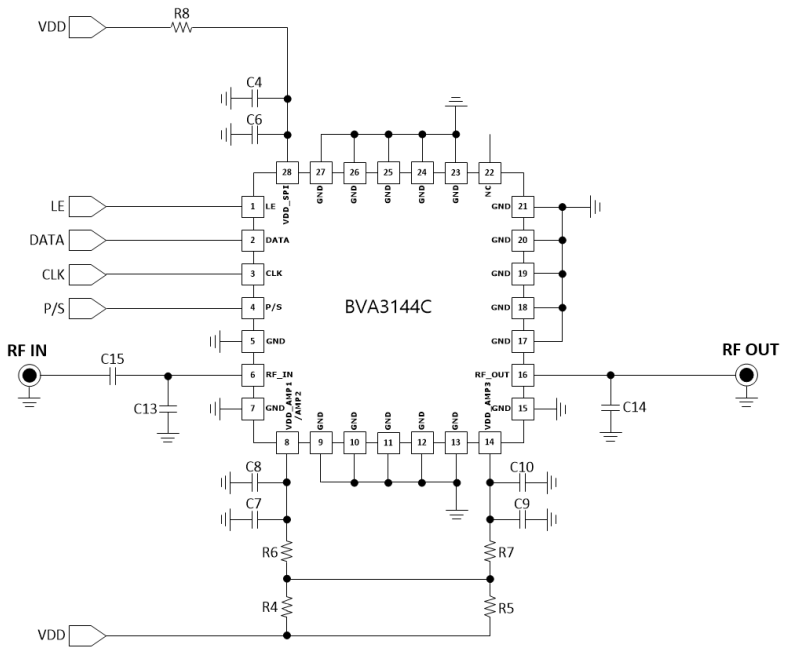


Typical RF Performance Plot - BVA3144C EVK - PCB

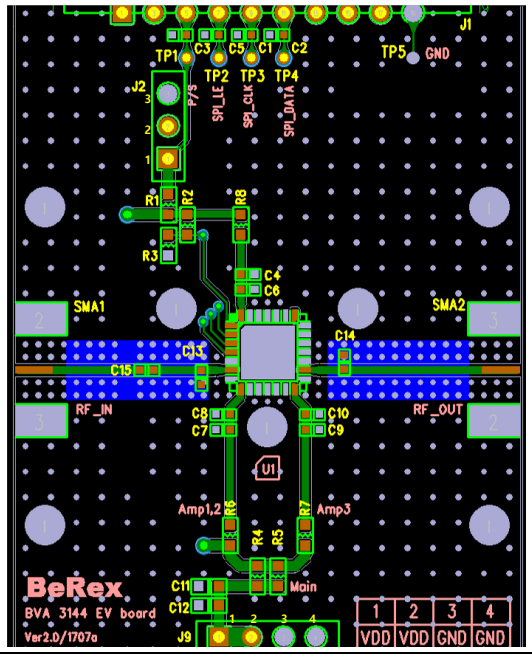
Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Table 9. Application Circuit

Schematic Diagram



BOM			Remark
Ref	Size	Value	
C4	0402	100 nF	
C6	0402	100 pF	
C7	0402	100 nF	
C8	0402	100 pF	
C9	0402	100 nF	
C10	0402	100 pF	
C13	0201	0.3 pF	
C14	0201	0.7 pF	
C15	0201	0.7 pF	
R4	0603	0 Ω	
R5	0603	0 Ω	
R6	0603	0 Ω	
R7	0603	0 Ω	
R8	0603	0 Ω	



NOTE

1. J1 Information
   - Pin 5 : P/S (TP1)
   - Pin 7 : LE (TP2)
   - Pin 9 : CLK (TP3)
   - Pin 11 : DATA (TP4)
   - Pin 19 : GND (TP5)
2. J2 Information
   - Not connected (Floating) : Serial Mode
   - Connected 1-2 : Serial Mode
   - Connected 2-3 : Bypass mode (Max Gain State)
3. J9 Information
   - Pin 1, 2 : 5Vdc
   - Pin 3, 4 : Ground

Typical RF Performance Plot - BVA3144C EVK - PCB

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Table 10. Typical Performance by Temperature[1] : 4.6GHz

parameter	Typical Values				Units
Temperature	-40	25	105	125	°C
VDD	5	5	5	5	V
Current	300	310	325	320	mA
Gain[2]	38.5	37.3	35.5	34.9	dB
S11	-11.2	-11.3	-11.0	-11.0	dB
S22	-14.6	-14.2	-13.4	-13.5	dB
OIP3[3]	39.0	40.0	39.3	37.8	dBm
P1dB	26.8	26.5	25.7	25.4	dBm
Noise Figure	3.5	4.2	5.2	5.3	dB
LTE20MHz ACP[4]	62.1	62.9	62.9	62.8	dBc
5GNR 100MHz ACP[5]	54.2	54.5	54.7	54.0	dBc

1. Above test parameters are measured at Max Gain State (ATT=0dB)
2. Gain data has PCB & Connectors insertion loss de-embedded.
3. OIP3 measured with two tones at an output of 5 dBm per tone separated by 1 MHz.
4. LTE set-up : 3GPP LTE, E-TM3.1, 20MHz BW, ±20MHz offset, PAR 9.6 at 0.01% Prob. Output power 7dBm. Applied the Noise correlation function of Instrument.
5. 5GNR set-up : 3GPP 5GNR, 100MHz BW, ±100MHz offset. Output Power 7dBm. Applied the Noise correlation function of Instrument.

Figure 7. Gain vs. Frequency
Over Temperature (Max Gain State)

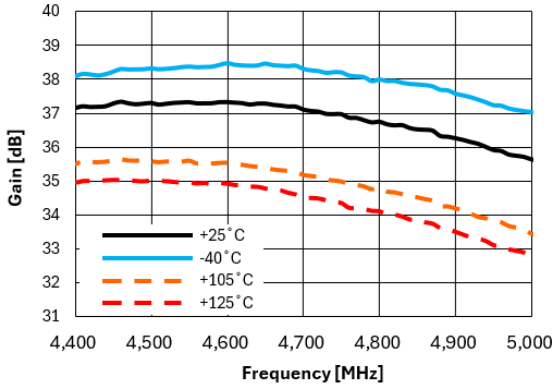
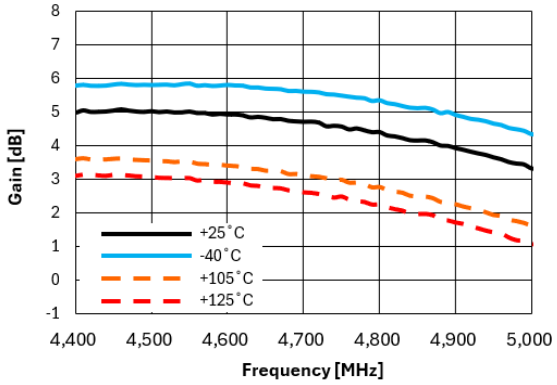
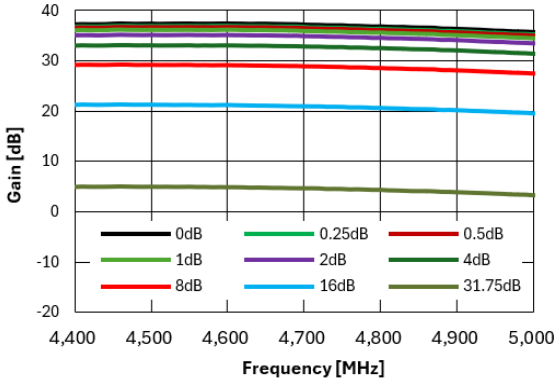


Figure 8. Gain vs. Frequency
Over Temperature (Min[1] Gain State)



1.Min Gain was measured in the state is set with attenuation 31.75dB.

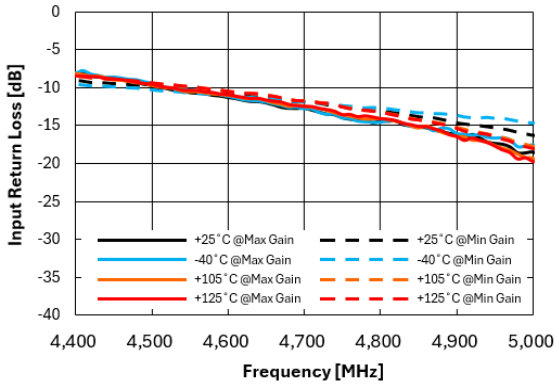
Figure 9. Gain vs. Frequency
Over Major Attenuation States



Typical RF Performance Plot - BVA3144C EVK - PCB

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Figure 10. Input Return Loss vs. Frequency
Over Temperature (Min[1] / Max Gain State)



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 11. Input Return Loss vs. Frequency
Over Major Attenuation States

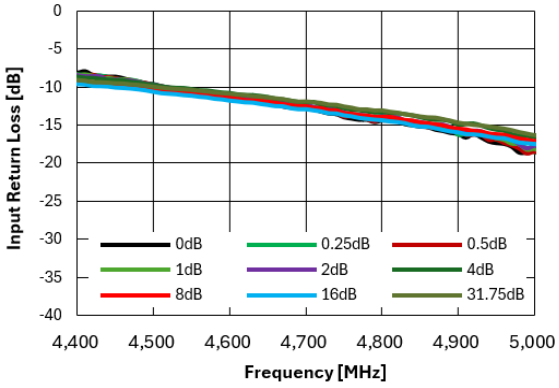
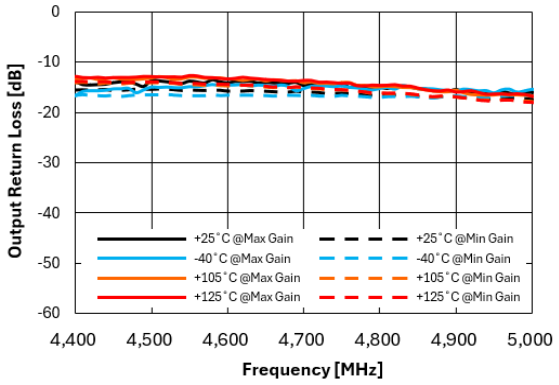
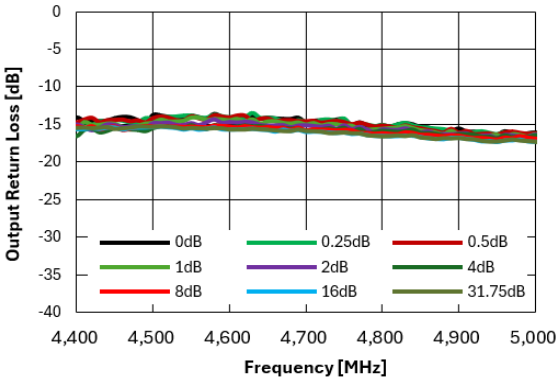


Figure 12. Output Return Loss vs. Frequency
Over Temperature (Min[1] / Max Gain State)



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 13. Output Return Loss vs. Frequency
Over Major Attenuation States



Typical RF Performance Plot - BVA3144C EVK - PCB

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Figure 14. Attenuation Error vs Frequency
Over Major Attenuation Steps

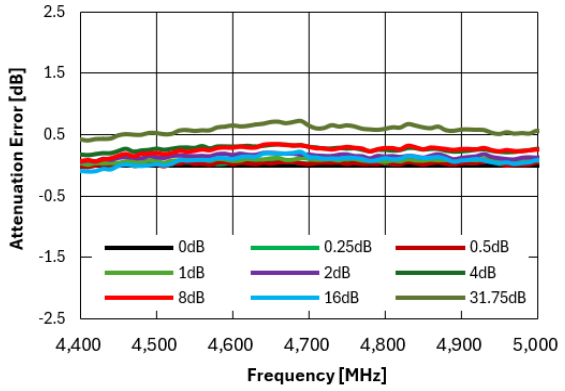


Figure 15. Attenuation Error vs Attenuation Setting
Over Major Frequency (Max Gain State)

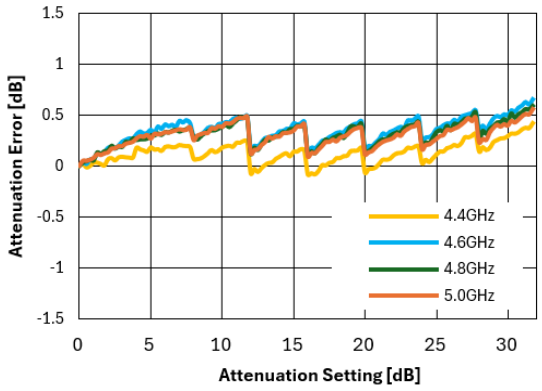


Figure 16. Attenuation Error at 4.4GHz vs Temperature
Over All Attenuation States

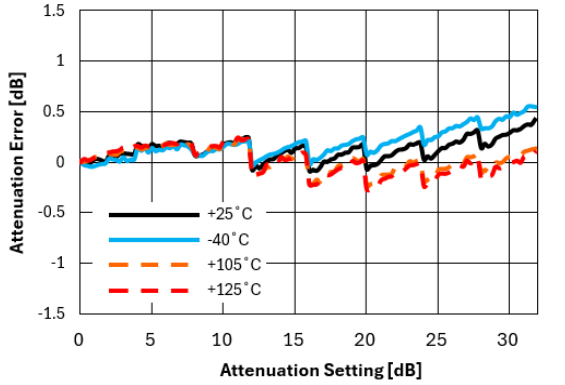


Figure 17. Attenuation Error at 4.6GHz vs Temperature
Over All Attenuation States

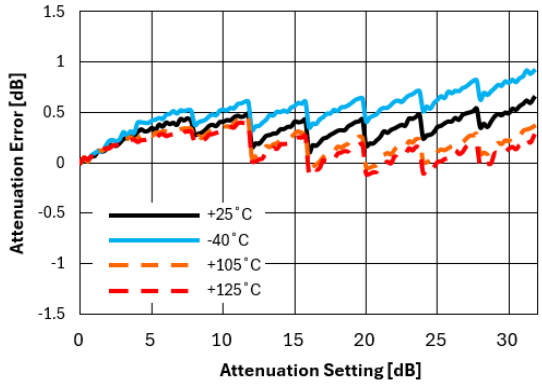


Figure 18. Attenuation Error at 4.8GHz vs Temperature
Over All Attenuation States

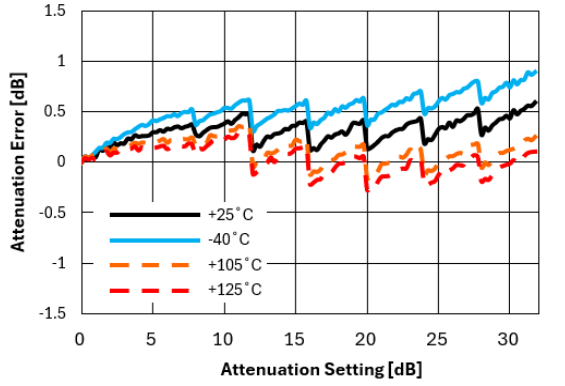
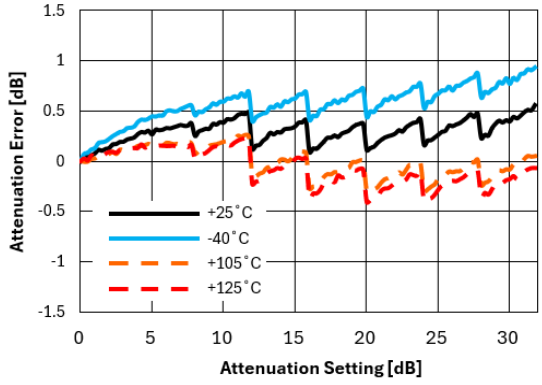


Figure 19. Attenuation Error at 5GHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA3144C EVK - PCB

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Figure 20. OIP3 vs. Frequency
Over Temperature (Max Gain State)

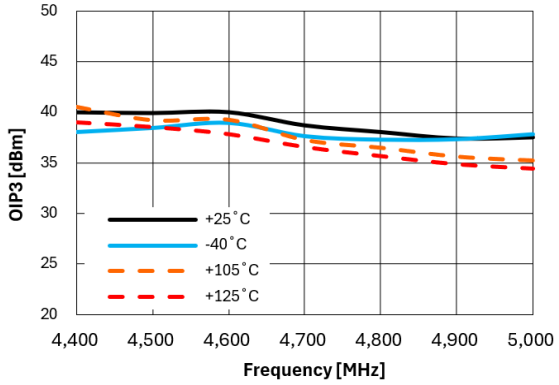


Figure 21. OIP3 vs. Frequency
Over Temperature (15.75dB Attenuation State)

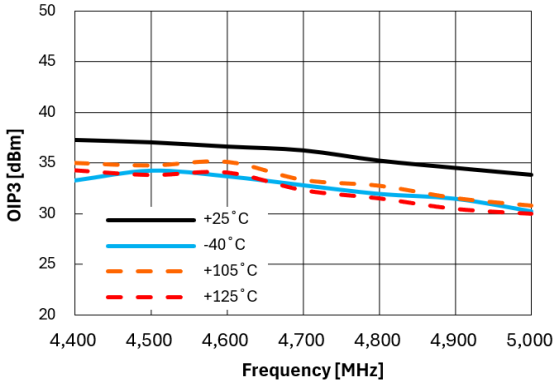


Figure 22. OP1dB vs. Frequency
Over Temperature (Max Gain State)

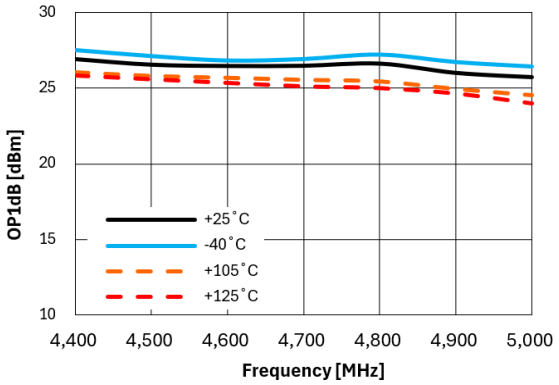
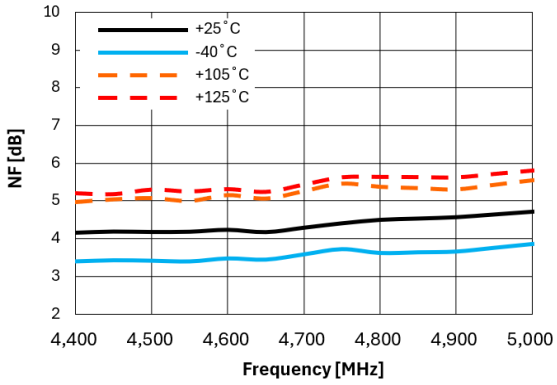


Figure 23. Noise Figure vs. Frequency
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA3144C EVK - PCB

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Figure 24. ACP vs. Pout
Over Major Frequency (Max Gain State), 5GNR 100MBW

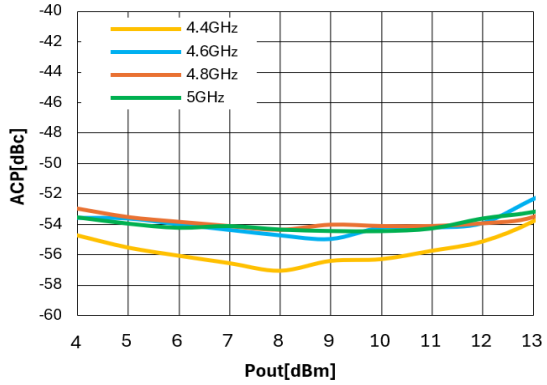


Figure 25. ACP vs. Pout
Over Major Frequency (15dB Attenuation State), 5GNR 100MBW

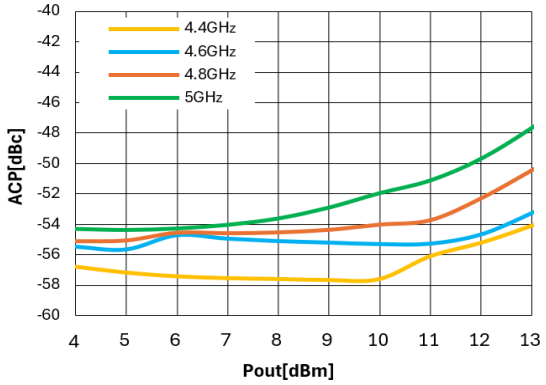


Figure 26. ACP at 4.6GHz vs. Pout
Over Temperature (Max Gain State), 5GNR 100MBW

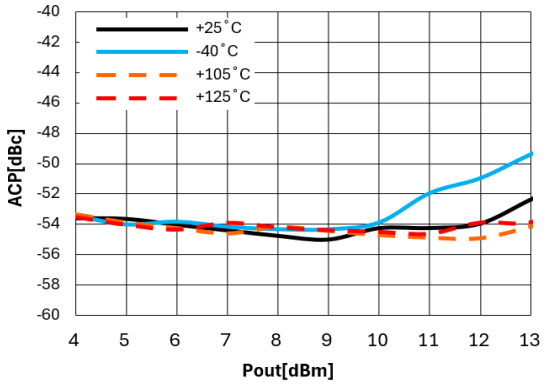


Figure 27. ACP Plot at 4.6GHz
5GNR 100MBW, 7dBm

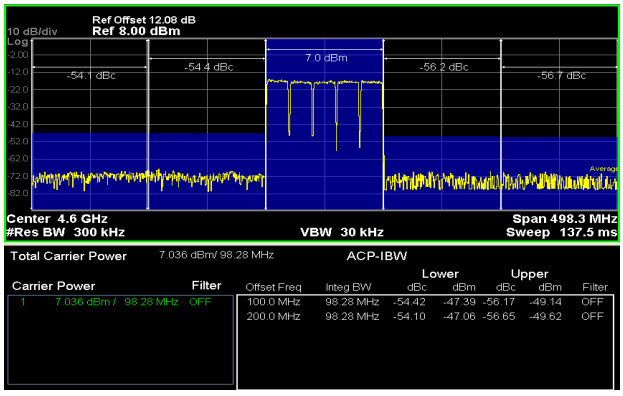


Figure 28. ACP Plot at 4.6GHz
5GNR 100MBW, 50dBc

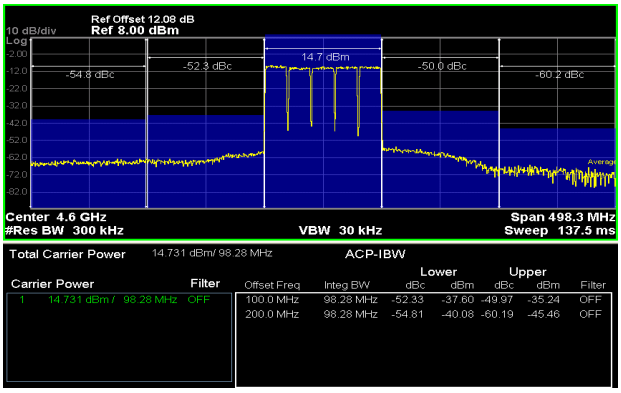


Figure 29. ACP Plot at 4.6GHz
LTE PAR 9.6dB 20MBW, 50dBc

Figure 30. Evaluation Board Schematic Diagram

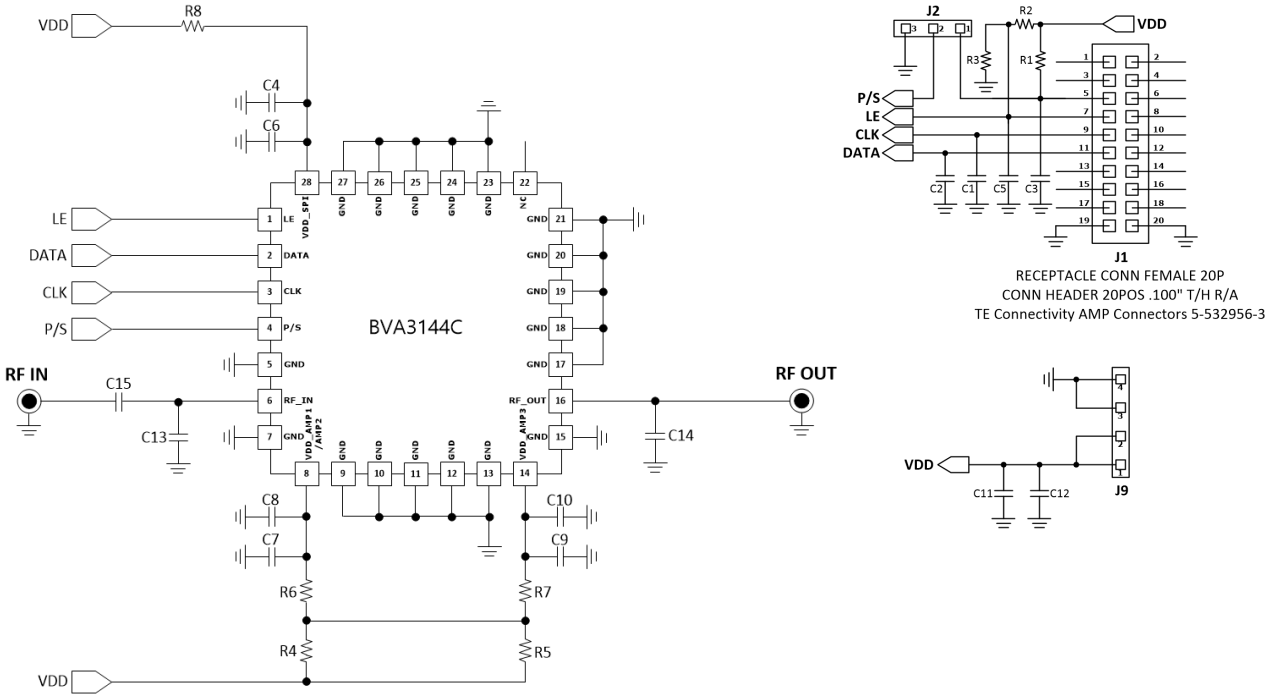


Figure 31. Evaluation Board PCB Layout Information

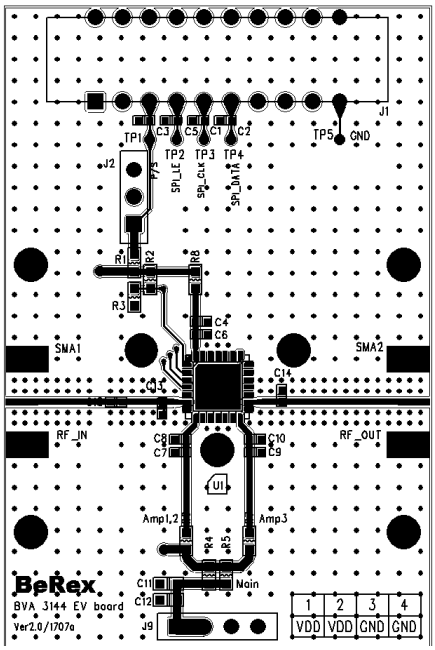


Table 11. Bill of Material - Evaluation Board

No.	Ref Des	Qty	Part Number	REMARK
1	R2	1	RES 0603 100kohm	
2	R3	1	RES 0603 200kohm	
3	R4, R5, R6, R7, R8	5	RES 0603 0ohm	
4	C4, C7, C9	3	CAP 0402 100nF	
5	C6, C8, C10	3	CAP 0402 100pF	
6	C11	1	CAP 0603 100pF	
7	C12	1	CAP 0603 1uF	
8	C13	1	CAP 0201 0.3pF	
9	C14, C15	2	CAP 0201 0.7pF	
10	U1	1	BVA3144C	SIP LGA 6x6 28Lead
11	SMA1, SMA2	2	SMA END LAUNCH	RF SMA Connector
12	J1	1	Receptacle connector 20pin	2.54mm, female
13	J2	1	3pin Header	2.54mm, male
14	J9	1	4pin Header	2.54mm, male
15	R1, C1, C2, C3, C5	5	NC	Not Connected

Figure 32. Suggested PCB Land Pattern and PAD Layout

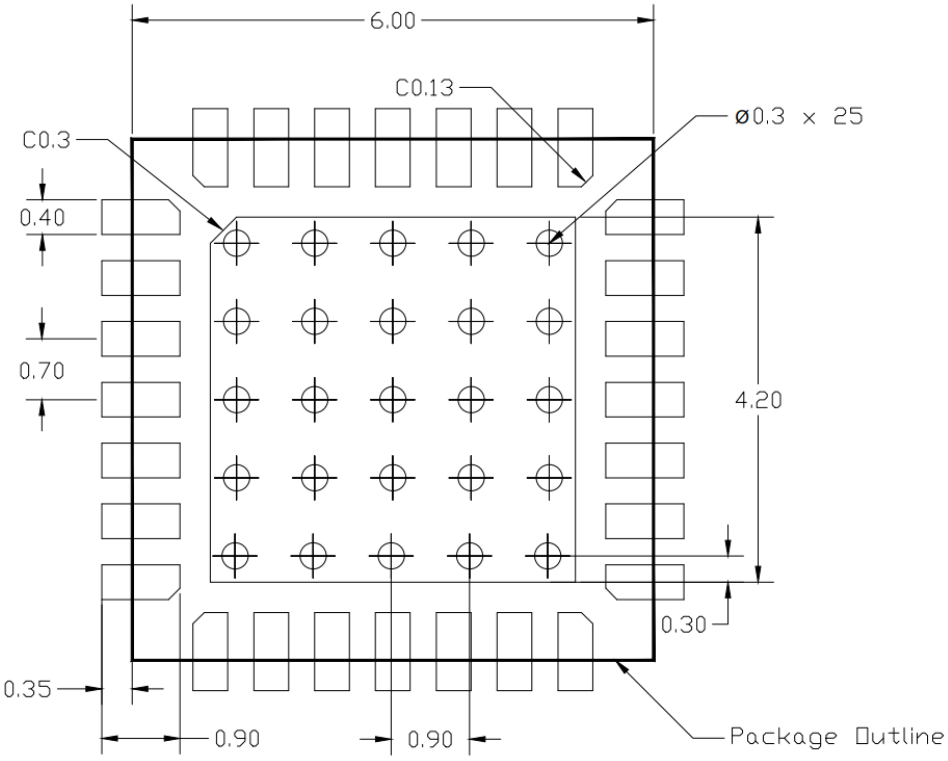


Figure 33. Evaluation Board PCB Layer Information

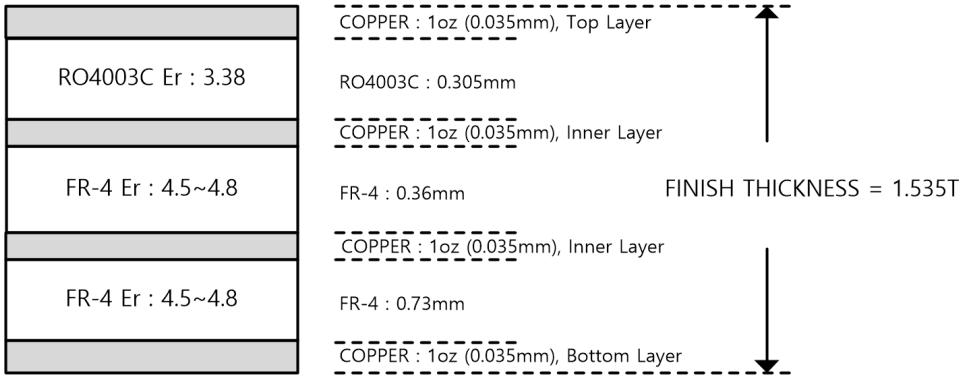
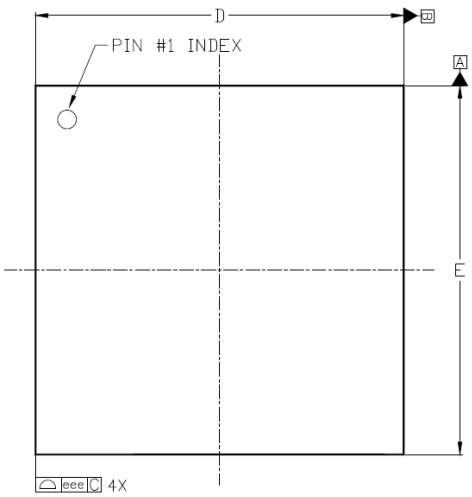
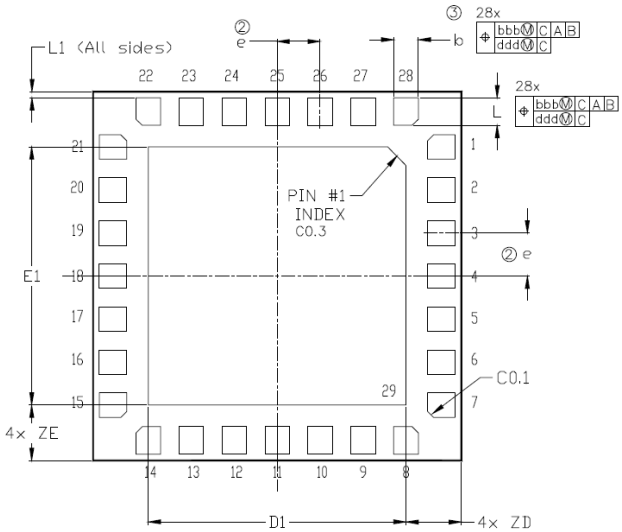


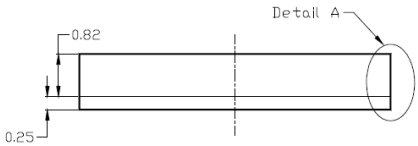
Figure 34. Package Outline Dimension



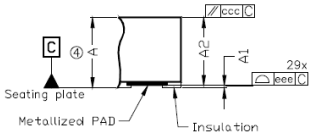
TOP VIEW



BOTTOM VIEW



SIDE VIEW



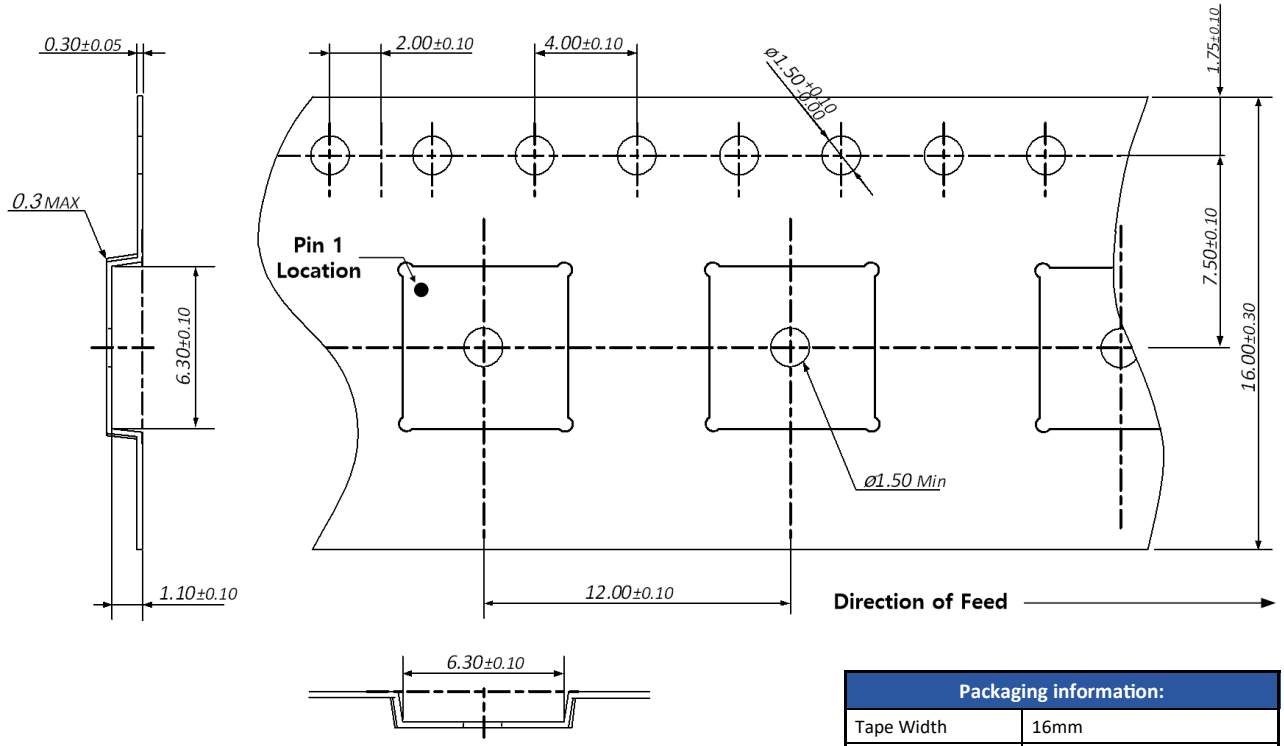
Detail A

Dimension Table				
Symbol Thickness	Min	Nominal	Max	Note
A	1.01	1.07	1.13	
A1	—	—	0.03	
A2	—	—	1.10	
b		0.40		
L		0.45		
L1	0.00	0.10	0.20	
D	5.90	6.00	6.10	
E	5.90	6.00	6.10	
D1		4.20 BSC		
ZD		0.90 BSC		
E1		4.20 BSC		
ZE		0.90 BSC		
aaa		0.10		
bbb		0.10		
ccc		0.10		
ddd		0.08		
eee		0.08		

NOTES:

1. All dimensions are in millimeters.
2. 'e1, e2' represents the basic terminal pitch. Specifies the true geometric position of the terminal axis.
3. Dimension 'b' applies to metallized terminal and is measured between 0.00mm and 0.25mm from terminal tip.
4. Diemstion 'A' inclueds package warpage.
5. Exposed metallized pads are cu pads with surface finish protection.
6. Package dimensions take reference to JEDEC MO-208 REV.C.

Figure 35. Tape and Reel



Packaging information:	
Tape Width	16mm
Reel Size	7”
Device Cavity Pitch	12mm
Devices Per Reel	1k

Figure 36. Package Marking

Marking information:	
BVA3144C	Device Name
YY	Year
WW	Work Week
XX	Wafer Lot Number

Lead Plating Finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

ESD / MSL Rating

ESD Rating :	Class 1C
Value :	±1000V
Test :	Human Body Model (HBM)
Standard :	JEDEC Standard JS-001-2017

ESD Rating :	Class C3
Value :	±1000V
Test :	Charged Device Model (CDM)
Standard :	JEDEC Standard JS-002-2018

MSL Rating :	MSL3 at +260°C convection reflow
Standard :	JEDEC Standard J-STD-020

Caution : ESD Sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Proper ESD procedures should be followed when handling the device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO GAGE Code :

2	N	9	6	F