BVA7202C

1/4W Flat Gain Digital Variable Gain Amplifier

400MHz – 1100MHz

Device Features

- Integrated AMP1 + DSA + AMP2
- A Single Voltage Supply : +5.0V / 165mA
- 0.4 - 1.1GHz Frequency Range
- 35.3dB Gain @ 0.9GHz
- Gain Flatness
  Under 1.1dB @ 700MBW (0.4 - 1.1GHz)
- 4.4dB Noise Figure @ 0.9GHz (Max gain)
- 23.4dBm Output P1dB @ 0.9GHz (Max gain)
- High Output IP3
  39.0dBm @ 0.9GHz , ATT 0dB (Max gain)
  35.6dBm @ 0.9GHz , ATT 15.5dB
- Attenuation: 0 - 31.5dB / 0.5 dB step
- Glitch-less attenuation state during transitions
- High attenuation accuracy
  ±(0.25 + 5% x ATT) @ 0.4 - 1.1GHz
- Serial Programming Interface only
- Power Down Mode (P/D)
- Lead-free/RoHS2-compliant 28-lead 6mm x 6mm x 1.07mm SIP LGA SMT Package

28-lead 6mm x 6mm x 1.07mm SIP LGA

Figure 1. Package Type

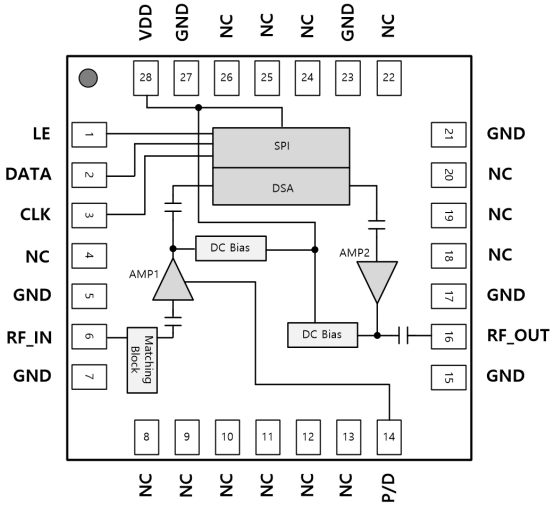


Figure 2. Functional Block Diagram

Product Description

The BVA7202C is a digitally controlled variable gain amplifier (DVGA) in a 6mm x 6mm SIP LGA package, with a frequency range of 0.4GHz to 1.1GHz at VDD of 5.0V.

The BVA7202C is a high performance and high dynamic range makes it ideally suited for use in LTE/3G/5G wireless infrastructure and other high performance wireless RF applications.

The BVA7202C is an integration of a high performance digital 6-bit attenuator (DSA) that provides a 31.5dB attenuation range in 0.5dB steps and two amplifiers. Two amplifiers in BVA7202C provide high OIP3 and OP1dB.

The BVA7202C supports digital control interface for serial programming of the Step attenuator (DSA) and has a power down feature for power savings with Power Down (P/D) mode.

This device is packaged in a 28-lead SIP LGA, 6mm x 6mm x 1.07mm with 50Ω single-ended RF input and RF output impedances for ease of integration into the signal-path.

The BVA7202C does not require blocking capacitors. If DC is presented at the RF port, add a blocking capacitor.

Application

- 5G/4G/3G wireless Infrastructure
- Small Cells
- Repeaters

Table 1. Electrical Specifications[1]

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			400		1100	MHz
Gain[2]		ATT = 0dB @ 400MHz		34.4		dB
		ATT = 0dB @ 700MHz		35.3		
		ATT = 0dB @ 900MHz		35.3		
		ATT = 0dB @ 1.1GHz		34.2		
Attenuation Control range		0.5dB Step		0 - 31.5		dB
Attenuation Step				0.5		dB
Attenuation Accuracy		Any bit or bit combination			±(0.25 + 5% of ATT setting)	dB
Return Loss	Input Return Loss	ATT = 0dB		-15		dB
	Output Return Loss			-20		
Output Power for 1dB Compression		ATT = 0dB @ 400MHz		24.0		dBm
		ATT = 0dB @ 700MHz		23.9		
		ATT = 0dB @ 900MHz		23.4		
		ATT = 0dB @ 1.1GHz		23.0		
Output Third Order Intercept Point[3]		ATT = 0dB @ 400MHz		39.6		dBm
		ATT = 0dB @ 700MHz		39.6		
		ATT = 0dB @ 900MHz		39.0		
		ATT = 0dB @ 1.1GHz		38.2		
Noise Figure		ATT = 0dB @ 400MHz		4.6		dB
		ATT = 0dB @ 700MHz		4.4		
		ATT = 0dB @ 900MHz		4.4		
		ATT = 0dB @ 1.1GHz		4.4		
DSA Switching time		50% CTRL(LE) to 90% or 10% RF		500	800	ns
AMP Switching time		50% CTRL(PWRDN) to 90% or 10% RF		150		ns
Impedance				50		Ω

1. Device performance : measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+5.0V.
2. Gain data has PCB & Connectors insertion loss de-embedded.
3. OIP3 measured with two tones at an output of 5dBm per tone separated by 1MHz.

Table 2. Typical RF Performance [1]

Parameter	Frequency				Unit
Frequency	**0.4**	**0.7**	**0.9**	**1.1**	**GHz**
Gain[2]	34.4	35.3	35.3	34.2	dB
S11	-15.9	-16.1	-13.7	-11.5	dB
S22	-22.9	-26.1	-13.5	-10.3	dB
OIP3[3]	39.6	39.6	39.0	38.2	dBm
OP1dB	24.0	23.9	23.4	23.0	dBm
Noise Figure	4.6	4.4	4.4	4.4	dB

1. Device performance : measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+5.0V.
2. Gain data has PCB & Connectors insertion loss de-embedded.
3. OIP3 measured with two tones at an output of +5dBm per tone separated by 1MHz.

Table 3. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage	AMP1, DSA, AMP2	-0.3		5.5	V
Supply Current	AMP1, DSA, AMP2			330	mA
Digital Input voltage	Control Pin (P/D)	-0.3		3.6	V
Maximum Input power	AMP1, DSA, AMP2			+15	dBm
Storage Temperature		-55		+150	℃
Junction Temperature				+150	℃

Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	AMP1 + DSA + AMP2	0.4		1.1	GHz
Supply Voltage (VDD)	AMP1, DSA, AMP2	4.75	5	5.25	V
Supply Current	AMP1 + DSA + AMP2	132	165	198	mA
	DSA + AMP2 (AMP1 Off)		85		mA
P/D control Voltage	P/D high (AMP1 Off)	1.17		5	V
	P/D low (AMP1 On)	0		0.63	V
DSA control Voltage	Digital input high	1.17		3.6	V
	Digital input low	-0.3		0.63	V
Operating Temperature	AMP1 + DSA + AMP2	-40		+125	˚C

Specifications are not guaranteed over all recommended operating conditions.

Table 5. Package Thermal Characteristics

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	41.5	°C/W

Figure 3. Pin Configuration (Top View)

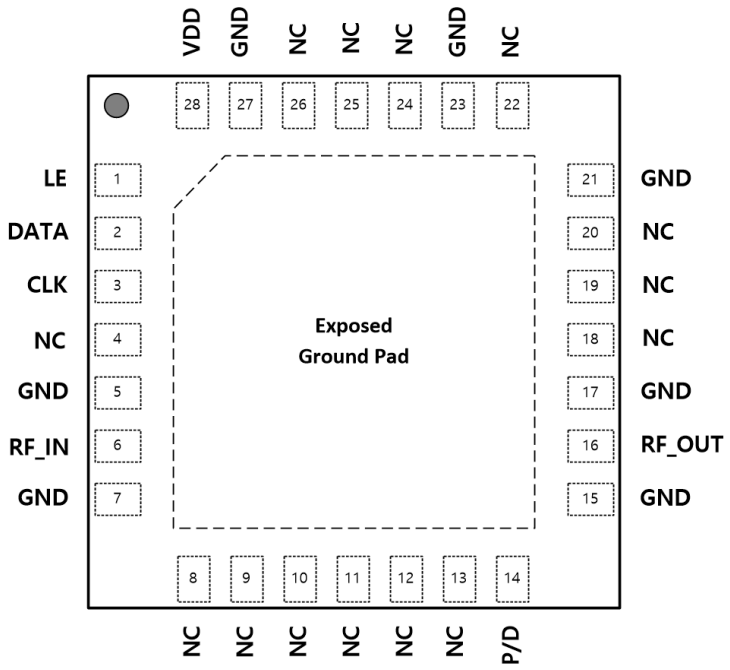


Table 6. Pin Description

Pin	Pin name	Description
1	LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial Data Input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial Clock Input.
6	RF_IN	RF input, matched to 50 ohm. Internally DC blocked.
14	P/D	VDD Power Down control Input. With Logic High(1.17 to 5V), Amplifier is Disabled. With Logic Low (0 to 0.63V), Amplifier is Enabled.
16	RF_OUT	RF output, matched to 50 ohm. Internally DC blocked.
28	VDD	SPI and DSA DC supply. This pin is connected to bypass capacitor internally.
4,8-13,18-20, 22,24-26	NC	Doesn't matter how these pins are NC (No Connection) or recommend connect to ground.
5,7,15,17, 21,23,27	GND	RF/DC Ground

Programming Option

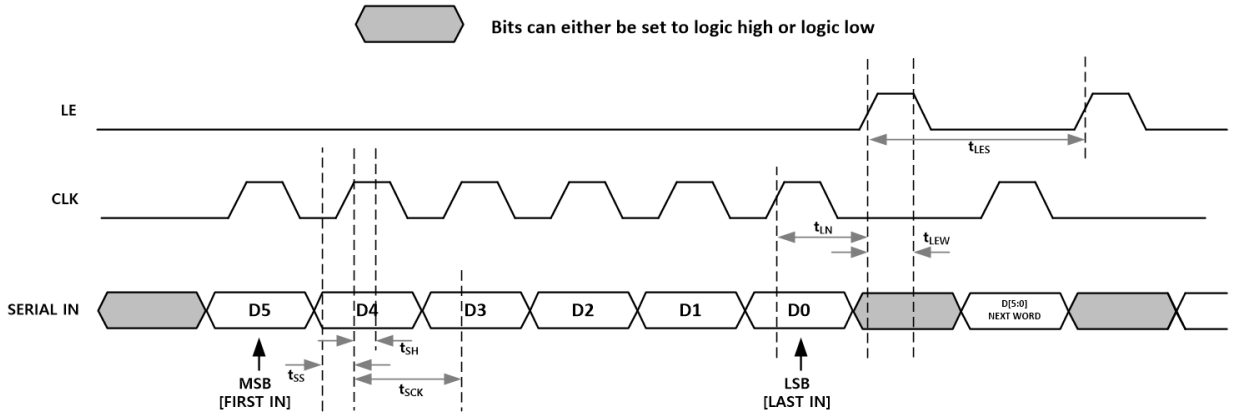
Programming Mode

The BVA7202C is only operating in Serial Mode.

Table 7. Truth Table for Serial Control Word

Digital Control Input						Attenuation State [dB]
D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	
0	0	0	0	0	0	0
0	0	0	0	0	1	0.5
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	1	0	0	0	4
0	1	0	0	0	0	8
1	0	0	0	0	0	16
1	1	1	1	1	1	31.5

Figure 4. Serial Interface Timing Diagram



Serial Interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The Attenuation Word truth table is listed in Table 7. The timing for this operation is defined by Figure 4 (Serial Interface Timing Diagram) and Table 8 (Serial Interface Timing Specifications).

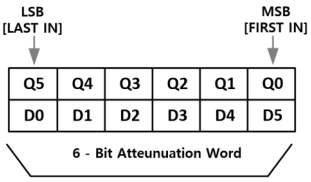
Table 8. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{CLK}	Serial data clock frequency			10	MHz
t_{SCK}	Minimum serial period	70			ns
t_{SS}	Serial Data setup time	10			ns
t_{SH}	Serial Data hold time	10			ns
t_{LN}	LE setup time	10			ns
t_{LEW}	Minimum LE pulse width	30			ns

Serial Register Map

The BVA7202C can be programmed via the serial control on the rising edge of Latch Enable (LE) which loads the last 6-bits data word in the SHIFT Register. Data is clocked in MSB(D5) first.

Figure 5. Serial Register Map



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by two, then convert to binary.
For example, to program the 15.5dB state :

2 x 15.5 = 31
D0 - D5 : 111110

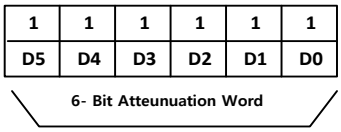
Serial Input : 111110

1	1	1	1	1	0
D0	D1	D2	D3	D4	D5

Power-UP states Settings

The BVA7202C always assumes a specifiable attenuation setting on power-up.
The BVA7202C is set to 31.5dB Attenuation setting by default on power-up. This attenuation setting is kept on until an initial serial control word is provided.

Figure 6. Default Attenuation word for Power-up state

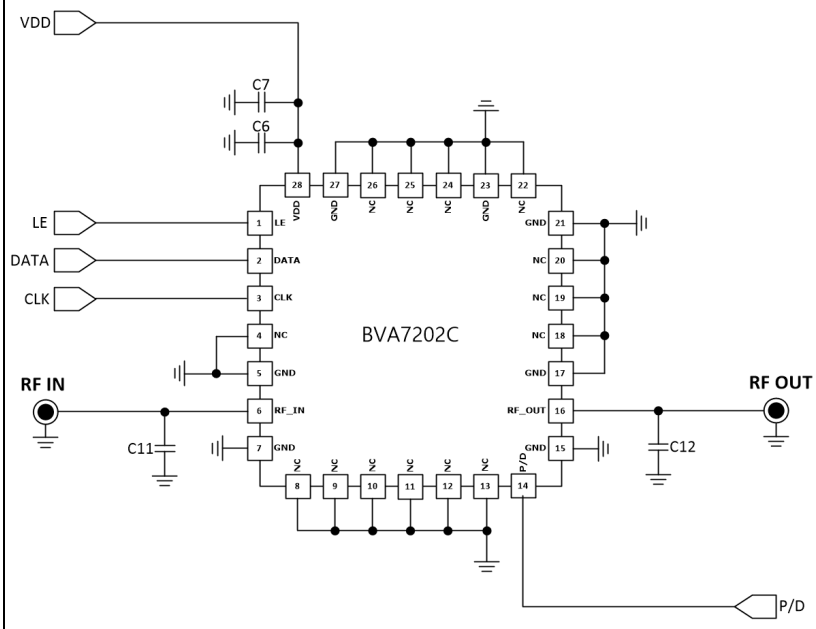


Typical RF Performance Plot - BVA7202C EVK - PCB

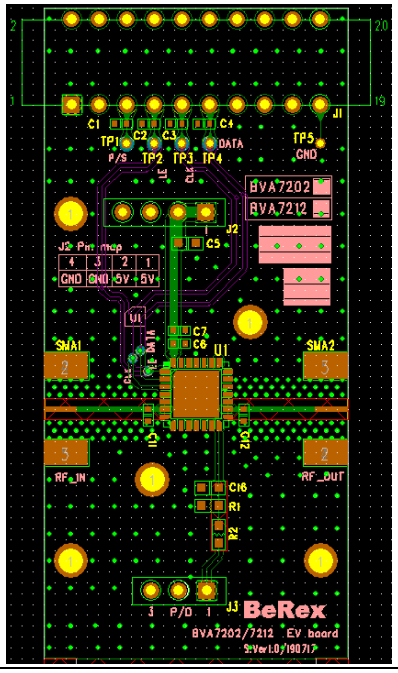
Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Table 9. Application Circuit

Schematic Diagram



BOM			Remark
Ref	Size	Value	
C6	0402	100 pF	
C7	0402	100 nF	
C11	0402	DNI	
C12	0402	DNI	



NOTE

1. J1 Information
   - Pin 5 : Not used. P/S (TP1)
   - Pin 7 : LE (TP2)
   - Pin 9 : CLK (TP3)
   - Pin 11 : DATA (TP4)
   - Pin 19 : GND (TP5)
2. J2 Information
   - Pin 1,2 : VDD pin
   - Pin 3,4 : GND
3. J3 Information
   - Pin 1 : P/D pin
   - Pin 2,3 : GND
   - Pin 1 Logic High AMP1 Disabled.
   - Pin 1 Logic Low AMP1 Enabled.

Typical RF Performance Plot - BVA7202C EVK - PCB

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Table 10. Typical Performance by Temperature[1] : 0.9GHz

Parameter	Typical Values				Units
Temperature	-40	25	105	125	°C
VDD	5	5	5	5	V
Current	167	165	160	156	mA
Gain[2]	36.2	35.3	33.8	33.4	dB
S11	-14.2	-13.7	-13.2	-13.2	dB
S22	-13.2	-13.5	-13.5	-13.3	dB
OIP3[3]	39.2	39.0	37.0	36.3	dBm
OP1dB	23.7	23.4	22.9	22.7	dBm
Noise Figure	3.7	4.4	5.2	5.5	dB

1. Above test parameters are measured at Max Gain State (ATT=0dB)
2. Gain data has PCB & Connectors insertion loss de-embedded.
3. OIP3 measured with two tones at an output of 5dBm per tone separated by 1MHz.

Figure 7. Gain vs. Frequency
Over Temperature (Max Gain State)

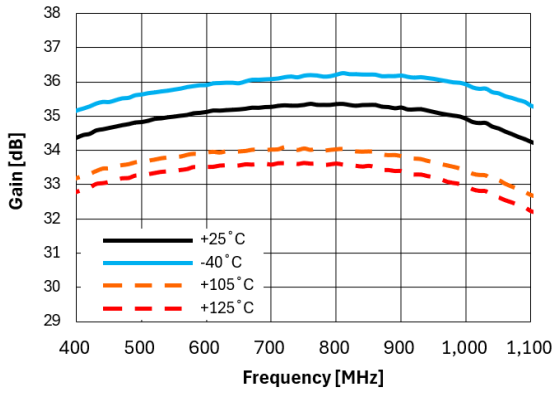
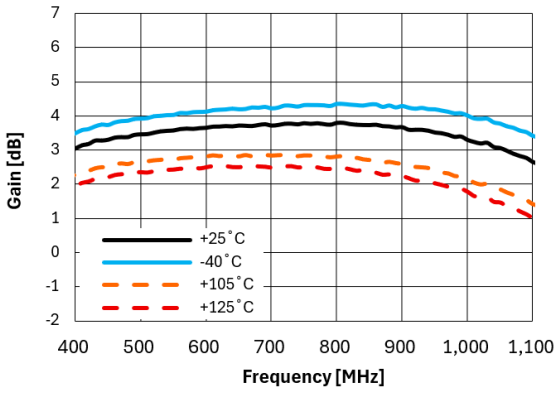
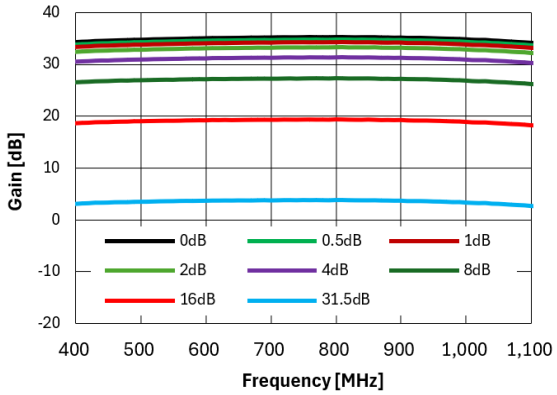


Figure 8. Gain vs. Frequency
Over Temperature (Min[1] Gain State)



1.Min Gain was measured in the state is set with attenuation 31.5dB.

Figure 9. Gain vs. Frequency
Over Major Attenuation States



Typical RF Performance Plot - BVA7202C EVK - PCB

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Figure 10. Input Return Loss vs. Frequency
Over Temperature (Min[1] / Max Gain State)

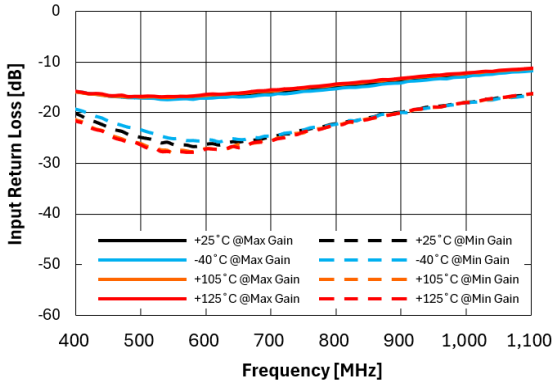
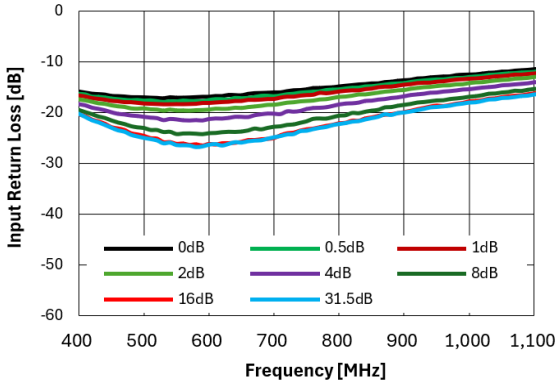


Figure 11. Input Return Loss vs. Frequency
Over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.5dB.

Figure 12. Output Return Loss vs. Frequency
Over Temperature (Min[1] / Max Gain State)

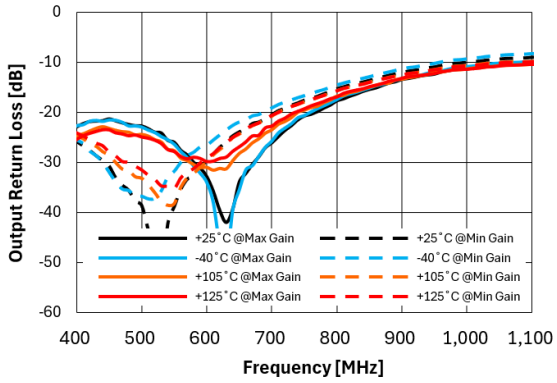
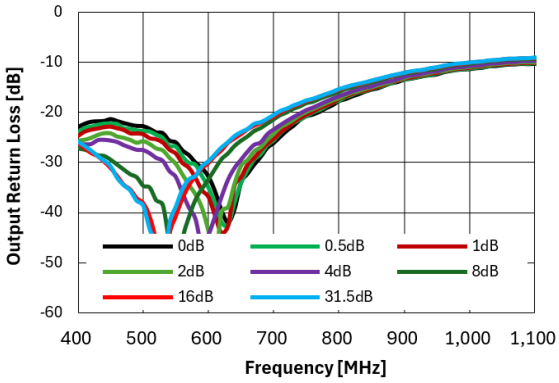


Figure 13. Output Return Loss vs. Frequency
Over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.5dB.

Typical RF Performance Plot - BVA7202C EVK - PCB

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Figure 14. Attenuation Error vs Frequency
Over Major Attenuation Steps

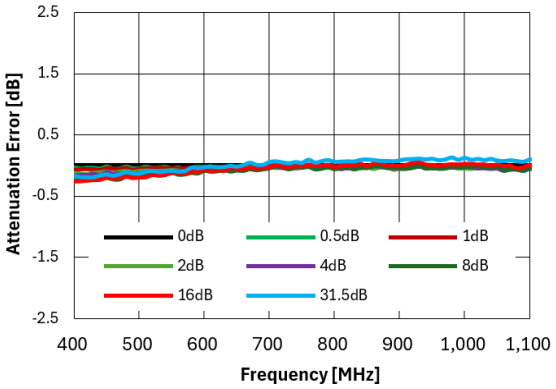


Figure 15. Attenuation Error vs Attenuation Setting
Over Major Frequency (Max Gain State)

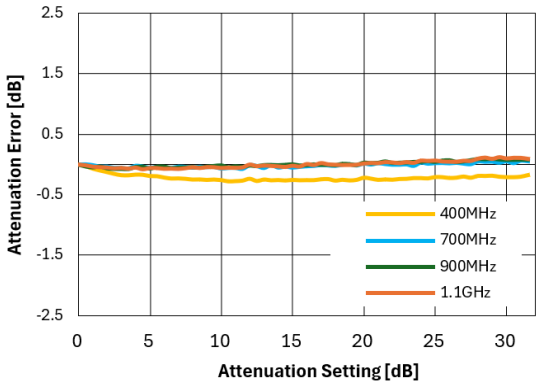


Figure 16. Attenuation Error at 400MHz vs Temperature
Over All Attenuation States

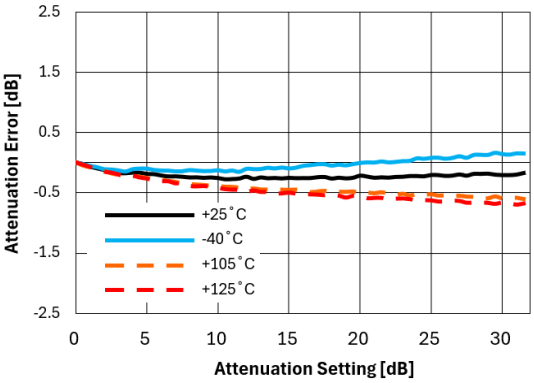


Figure 17. Attenuation Error at 700MHz vs Temperature
Over All Attenuation States

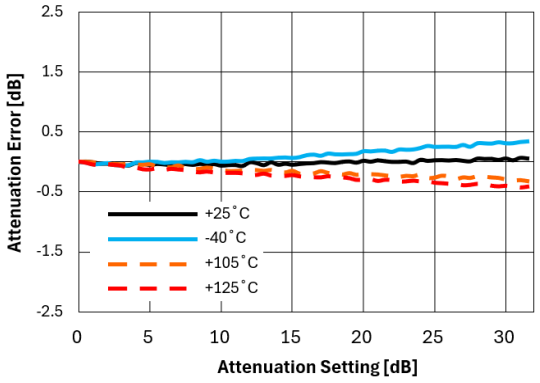


Figure 18. Attenuation Error at 900MHz vs Temperature
Over All Attenuation States

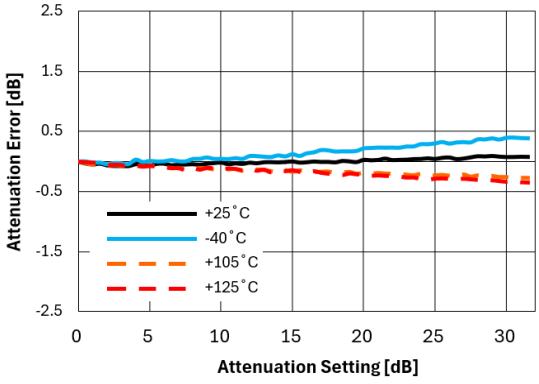
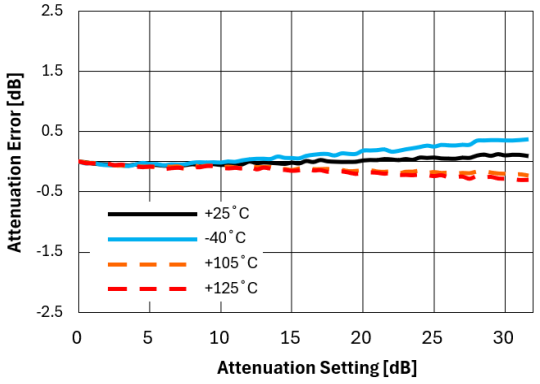


Figure 19. Attenuation Error at 1.1GHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA7202C EVK - PCB

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Figure 20. OIP3 vs. Frequency
Over Temperature (Max Gain State)

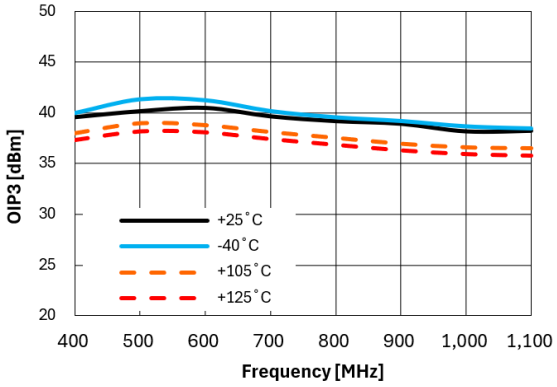


Figure 21. OIP3 vs. Frequency
Over Temperature (15.5dB Attenuation State)

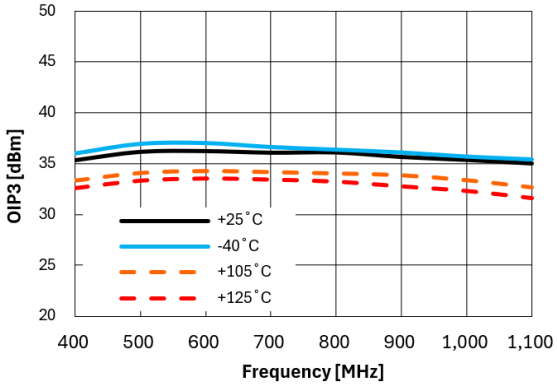


Figure 22. OP1dB vs. Frequency
Over Temperature (Max Gain State)

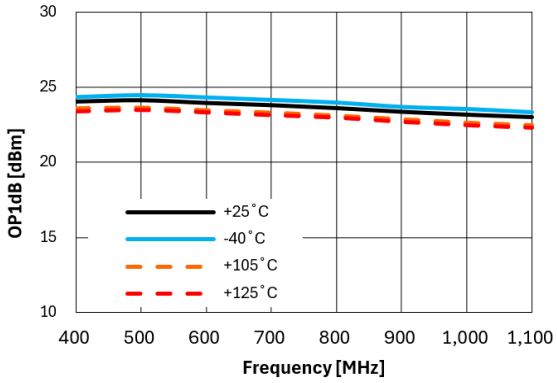
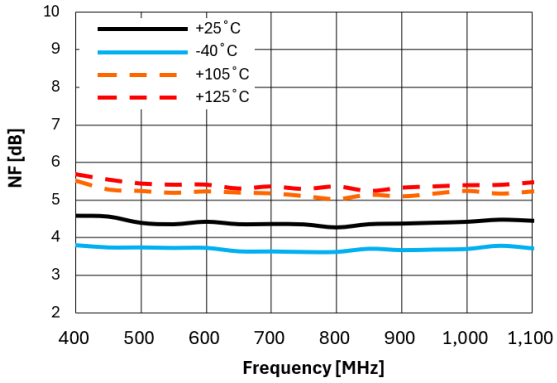


Figure 23. Noise Figure vs. Frequency
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA7202C EVK - PCB

Typical Performance Data @ 25°C and VDD = 5.0V unless otherwise noted.

Figure 24. Power On/Off Time
Rising Time (Control 50% to RF 90%)

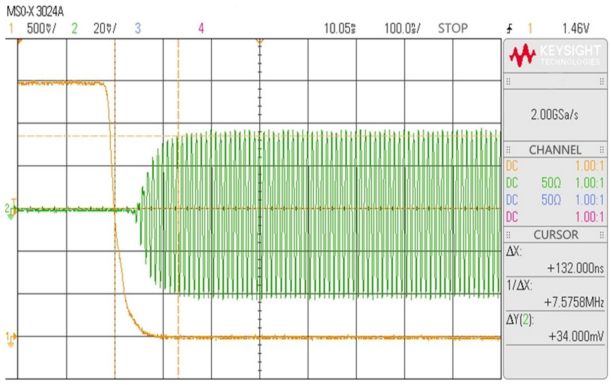


Figure 25. Power On/Off Time
Falling Time (Control 50% to RF 10%)

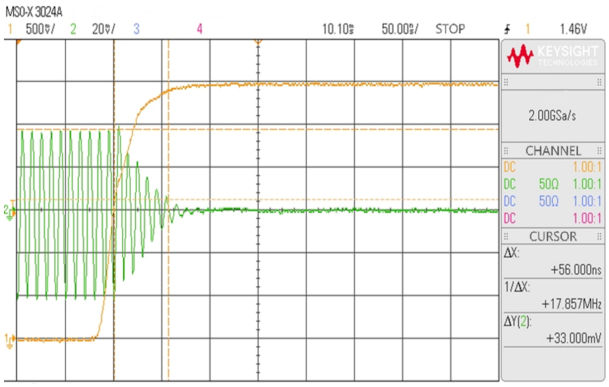


Figure 26. ACP Plot at 900MHz
LTE PAR 9.6dB 20MBW, 50dBc

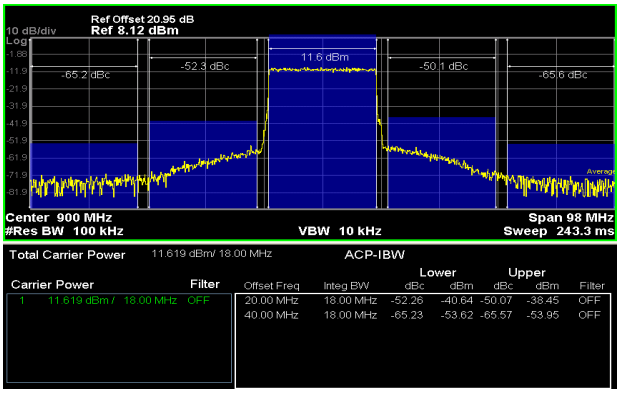


Figure 27. Evaluation Board Kit Schematic Diagram

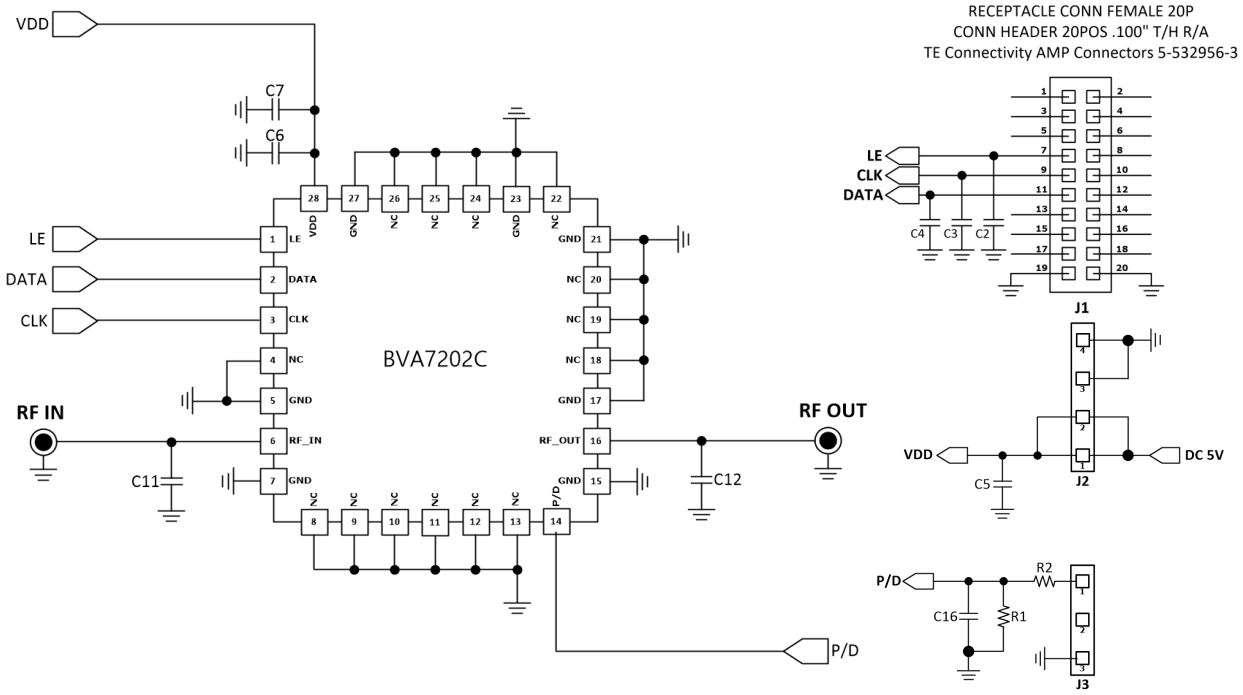


Figure 28. Evaluation Board PCB Layout Information

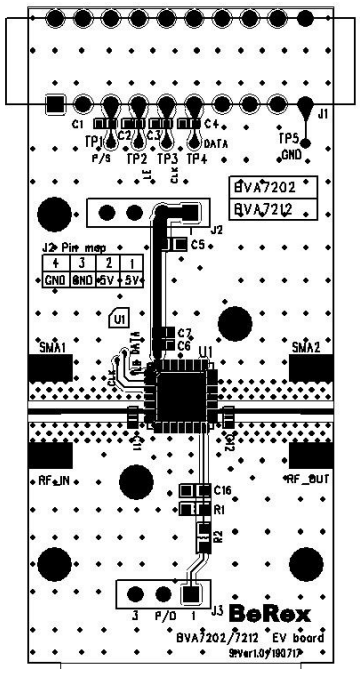


Table 11. Bill of Material - Evaluation Board

No.	Ref Des	Qty	Part Number	REMARK
1	R2	1	RES 0603 0ohm	
2	C6	1	CAP 0402 100pF	
3	C7	1	CAP 0402 100nF	
4	U1	1	BVA7202C	SIP LGA 6x6 28Lead
5	SMA1, SMA2	2	SMA END LAUNCH	RF SMA Connector
6	J1	1	Receptacle connector 20pin	2.54mm, female
7	J2	1	4pin Header	2.54mm, male
8	J3	1	3pin Header	2.54mm, male
9	R1, C1, C2, C3, C4, C5, C11, C12, C16	9	NC	Not Connected

RF Input was matched by Inductor internally. So that it needs DC Blocking Capacitors when DC voltage is presented at RF input port.

Figure 29. Suggested PCB Land Pattern and PAD Layout

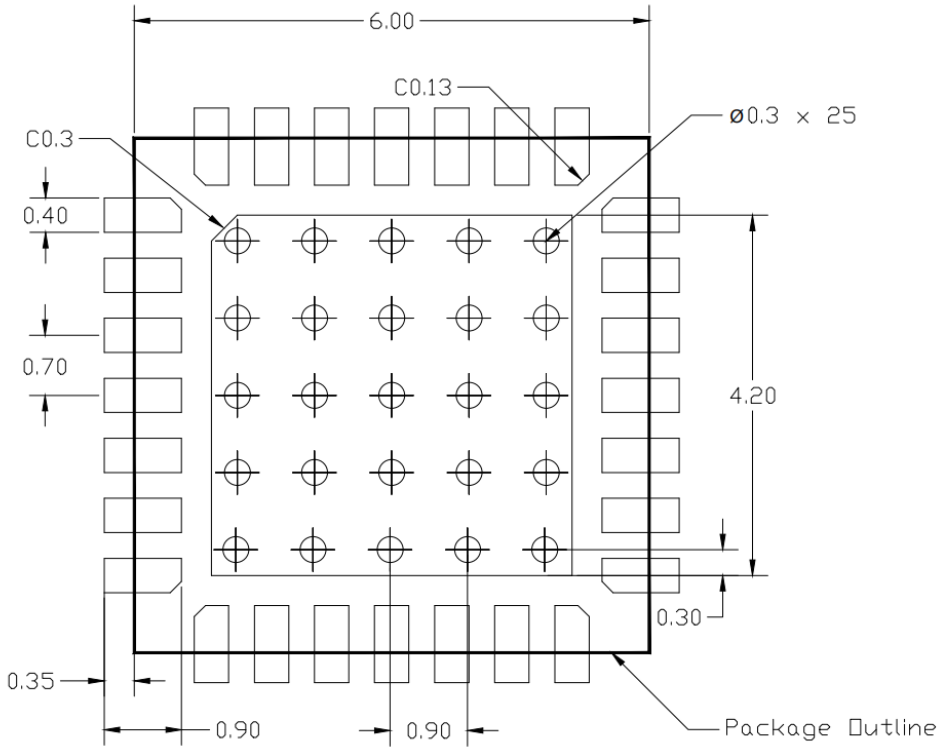


Figure 30. Evaluation Board PCB Layer Information

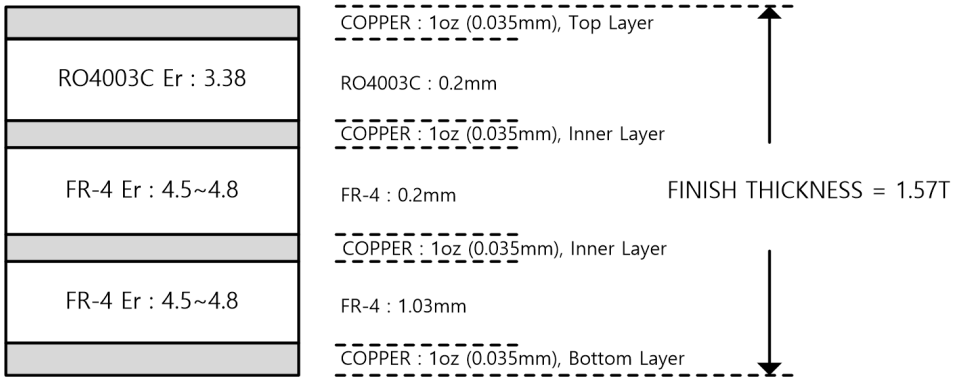
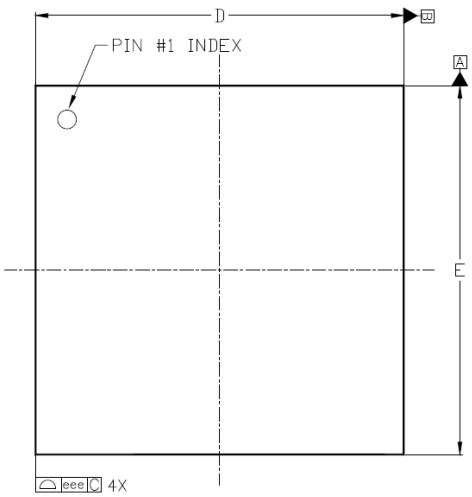
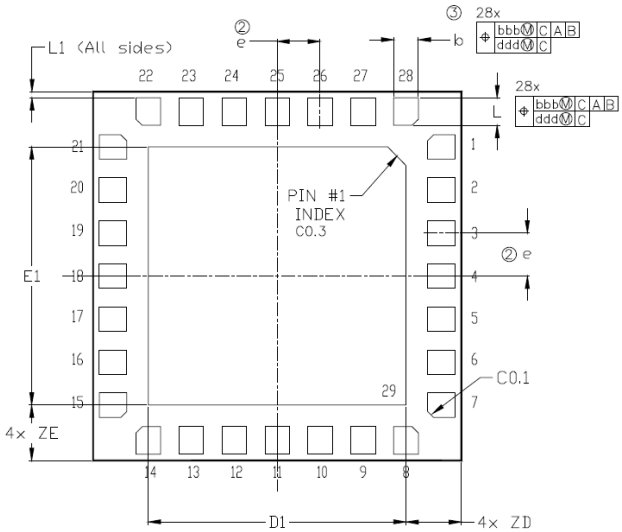


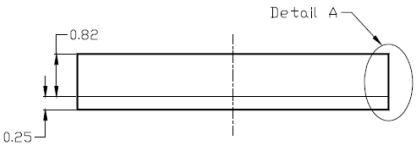
Figure 31. Package Outline Dimension



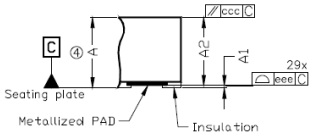
TOP VIEW



BOTTOM VIEW



SIDE VIEW



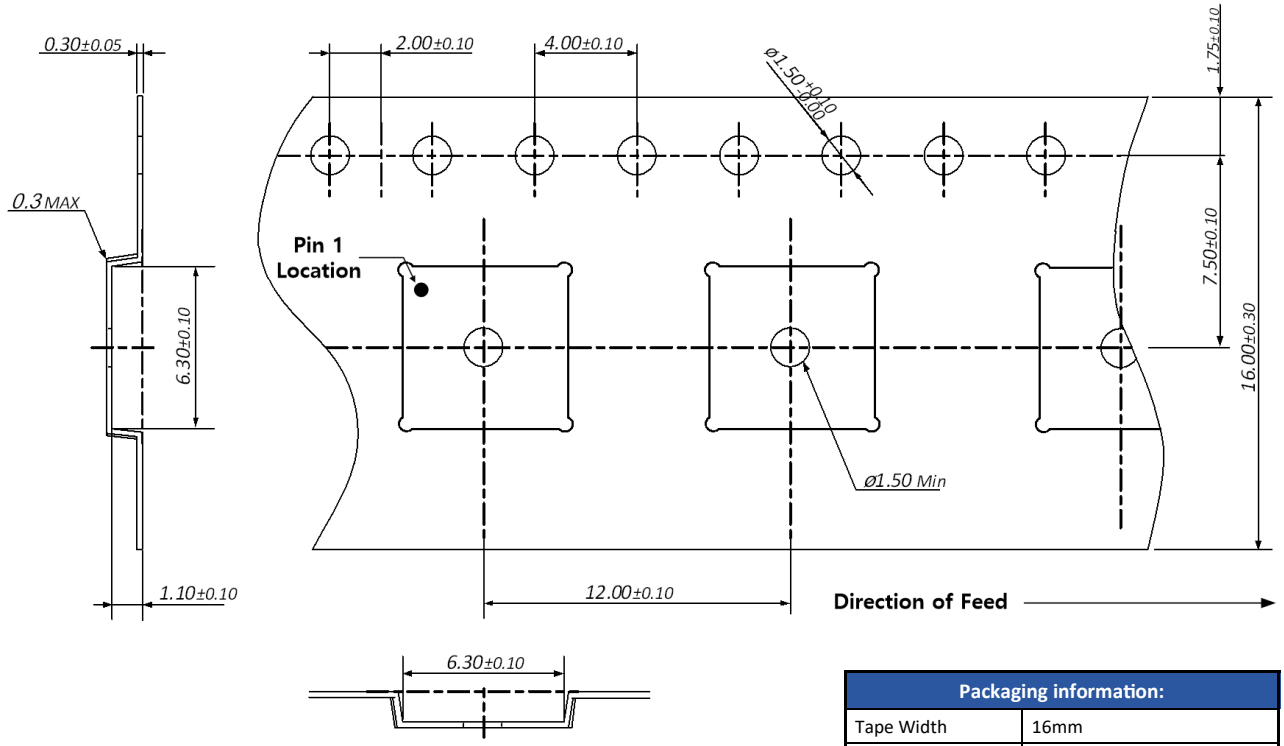
Detail A

Dimension Table				
Symbol Thickness	Min	Nominal	Max	Note
A	1.01	1.07	1.13	
A1	—	—	0.03	
A2	—	—	1.10	
b		0.40		
L		0.45		
L1	0.00	0.10	0.20	
D	5.90	6.00	6.10	
E	5.90	6.00	6.10	
D1	4.20 BSC			
ZD	0.90 BSC			
E1	4.20 BSC			
ZE	0.90 BSC			
aaa	0.10			
bbb	0.10			
ccc	0.10			
ddd	0.08			
eee	0.08			

NOTES:

1. All dimensions are in millimeters.
2. 'e1, e2' represents the basic terminal pitch. Specifies the true geometric position of the terminal axis.
3. Dimension 'b' applies to metallized terminal and is measured between 0.00mm and 0.25mm from terminal tip.
4. Diemstion 'A' inclueds package warpage.
5. Exposed metallized pads are cu pads with surface finish protection.
6. Package dimensions take reference to JEDEC MO-208 REV.C.

Figure 32. Tape and Reel



Packaging information:	
Tape Width	16mm
Reel Size	7”
Device Cavity Pitch	12mm
Devices Per Reel	1k

Figure 33. Package Marking

Marking information:	
BVA7202C	Device Name
YY	Year
WW	Work Week
XX	Wafer Lot Number

Lead Plating Finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

ESD / MSL Rating

ESD Rating :	Class 1C
Value :	±1000V
Test :	Human Body Model (HBM)
Standard :	JEDEC Standard JS-001-2017

ESD Rating :	Class C3
Value :	±1000V
Test :	Charged Device Model (CDM)
Standard :	JEDEC Standard JS-002-2018

MSL Rating :	MSL3 at +260°C convection reflow
Standard :	JEDEC Standard J-STD-020

Caution : ESD Sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Proper ESD procedures should be followed when handling the device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO GAGE Code :

2	N	9	6	F