

### Product Description

The BVA7212 is a digitally controlled variable gain amplifier (DVGA) in a 6mm x 6mm LGA package, with a frequency range of 1.4GHz to 2.3GHz at VDD of 5.0V.

The BVA7212 is a high performance and high dynamic range makes it ideally suited for use in LTE/3G/5G wireless infrastructure and other high performance wireless RF applications.

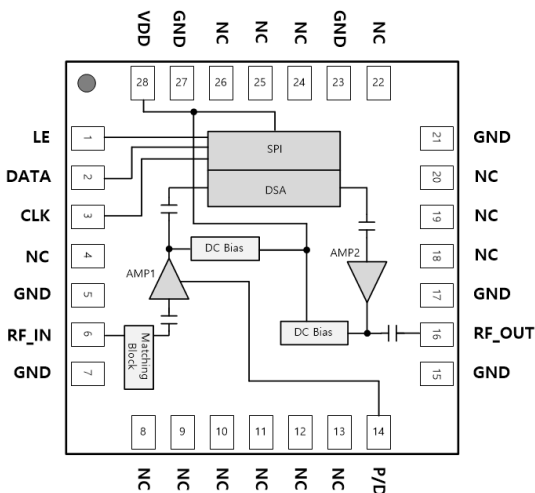
The BVA7212 is an integration of a high performance digital 6-bit attenuator (DSA) that provides a 31.5dB attenuation range in 0.5dB steps and two amplifiers. Two amplifiers in BVA7212 provide high OIP3 and OP1dB.

The BVA7212 digital control interface supports serial programming of the Step attenuator (DSA) and has a power down feature for power savings with Power Down (P/D) mode.

This device is packaged in a 28-pin LGA, 6mm x 6mm x 0.95mm with 50Ω single-ended RF input and RF output impedances for ease of integration into the signal-path.

The BVA7212 does not require blocking capacitors. If DC is presented at the RF port, add a blocking capacitor.

### Figure 1. Functional Block Diagram



### Figure 2. Package Type



28-pin 6mm x 6mm x 0.95mm LGA

### Device Features

- 28-pin 6mm x 6mm x 0.95mm LGA Package
- Integrated AMP1 + DSA + AMP2
- A Single Voltage Supply : +5.0V / 180mA
- 1.4 - 2.3GHz Frequency Range
- 33.2dB Gain @ 1.8GHz
- Gain Flatness
  - Under 1.0dB @ 900MHz BW (1.4 - 2.3GHz)
  - Under 0.5dB @ 400MHz BW (1.8 - 2.2GHz)
- 3.3dB Noise Figure @ 1.8GHz (Max gain)
- 24dBm Output P1dB @ 1.8GHz (Max gain)
- High Output IP3
  - 40.5dBm @ 1.8GHz, ATT 0dB (Max gain)
  - 40.1dBm @ 1.8GHz, ATT 6dB
  - 32.4dBm @ 1.8GHz, ATT 20dB
- Attenuation Range
  - 0 - 31.5dB / 0.5 dB step
- Glitch-less attenuation state during transitions
- High attenuation accuracy
  - ±(0.25dB + 6% x Atten) @ 1.4 - 2.3GHz
- Serial Programming Interface only
- Power Down Mode (P/D)
- Lead-free/RoHS2-compliant SiP LGA SMT Package

### Application

- 5G/4G/3G wireless Infrastructure
- Small Cells
- Repeaters

**Table 1. Electrical Specifications**

Typical Performance Data @ 25°C and VDD = 5.0V, ATT = 0dB state (Max gain) unless otherwise noted.  
(De-embedded PCB and connector Loss)

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			1.4		2.3	GHz
Gain		ATT = 0dB, @ 1.8GHz	30.7	33.2	35.7	dB
Gain Flatness		1.8GHz to 2.2GHz		0.5		dBpp
		1.4GHz to 2.3GHz		1.0		dBpp
Attenuation Control range		0.5dB step			31.5	dB
Attenuation Step				0.5		dB
Attenuation Accuracy		Any bit or bit combination	- (0.25 +6% of ATT. setting)		+ (0.25 +6% of ATT. setting)	dB
Return loss	Input Return Loss	Attenuation = 0dB		15		dB
	Output Return Loss			12		
Output Power for 1dB Compression		ATT = 0dB, @ 1.8GHz		24		dBm
Output Third Order Intercept Point		ATT = 0dB, @ 1.8GHz Pout= 7dBm/tone $\Delta f=1$ MHz	36	40.5		dBm
		ATT= 20dB, @ 1.8GHz Pin= -20dBm/tone $\Delta f=1$ MHz		32.4		dBm
Noise Figure		ATT = 0dB, @ 1.8GHz		3.3		dB
DSA Switching time		50% CTRL to 90% or 10% RF		500	800	ns
Power Down (P/D) Switching time		50% CTRL to 90% or 10% RF		150		ns
Supply voltage		AMP1, DSA, AMP2		5		V
Supply Current		AMP1, DSA, AMP2	144	180	216	mA
DSA control Voltage		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.63	V
P/D control Voltage		P/D high (AMP1 Off)	1.17		5	V
		P/D low (AMP1 On)	0		0.63	V
		Current(AMP2) @ P/D High (AMP1 off)		90		mA
Impedance				50		$\Omega$

**Table 2. Typical RF Performance<sup>1</sup>**

Parameter	Frequency					Unit
	1.4	1.6	1.8	2.1	2.3	
Frequency	1.4	1.6	1.8	2.1	2.3	GHz
Gain	32.7	33.0	33.2	33.6	33.3	dB
S11	-17.8	-16.8	-15.3	-19.9	-23.1	dB
S22	-9.4	-11.0	-12.6	-12.4	-8.7	dB
OIP3 <sup>2</sup> (Max Gain, ATT=0dB)	42	41.8	40.6	39.6	39.1	dBm
OIP3 <sup>2</sup> (ATT=20dB)	30.8	32.2	32.5	32.1	31.7	dBm
OP1dB	23.9	23.7	23.6	23.9	24.2	dBm
N.F (Max Gain, ATT=0dB)	3.4	3.3	3.3	3.4	3.5	dB
N.F (ATT=20dB)	11.4	10.9	10.6	10.4	10.7	dB

<sup>1</sup> Device performance measured on a BeRex evaluation board at 25°C, VDD=+5.0V, 50 Ω system. measure on Evaluation Board De-embedded PCB and Connector Loss.

<sup>2</sup> OIP3 measured with two tones at an output of +7dBm per tone separated by 1MHz.

**Table 3. Absolute Maximum Ratings<sup>1</sup>**

Parameter	Min	Typ	Max	Unit
Supply Voltage (VDD)	-0.3		5.5	V
Digital input voltage	-0.3		3.6	V
Maximum input power			+15	dBm
Storage Temperature	-55		+150	°C
Junction Temperature			+160	°C

<sup>1</sup> Operation of this device above any of these parameters may result in permanent damage.

**Table 4. Recommended Operating Conditions<sup>1</sup>**

Parameter	Min	Typ	Max	Unit
Frequency Range	1.4		2.3	GHz
Supply Voltage (VDD)	4.75	5	5.25	V
Operating Temperature	-40		+105	°C
Thermal Resistance R <sub>TH</sub> (θ <sub>JA</sub> )		41.4		°C/W

<sup>1</sup> Specifications are not guaranteed over all recommended operating conditions.

### Programming Option

#### Programming Mode

The BVA7212 is only operating in Serial Mode.

#### Serial Interface

The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 4 (Serial Interface Timing Diagram) and Table 6 (Serial Interface AC Characteristics).

#### Power-up Control Settings

The BVA7212 always assumes a specifiable attenuation setting on power-up.

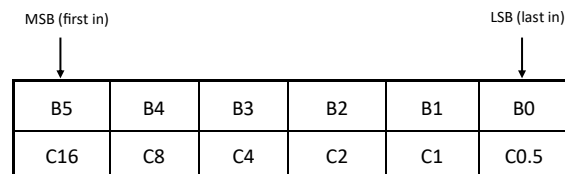
The BVA7212 is set to 28dB Attenuation setting by default on power-up. This attenuation setting is kept on until an initial serial control word is provided.

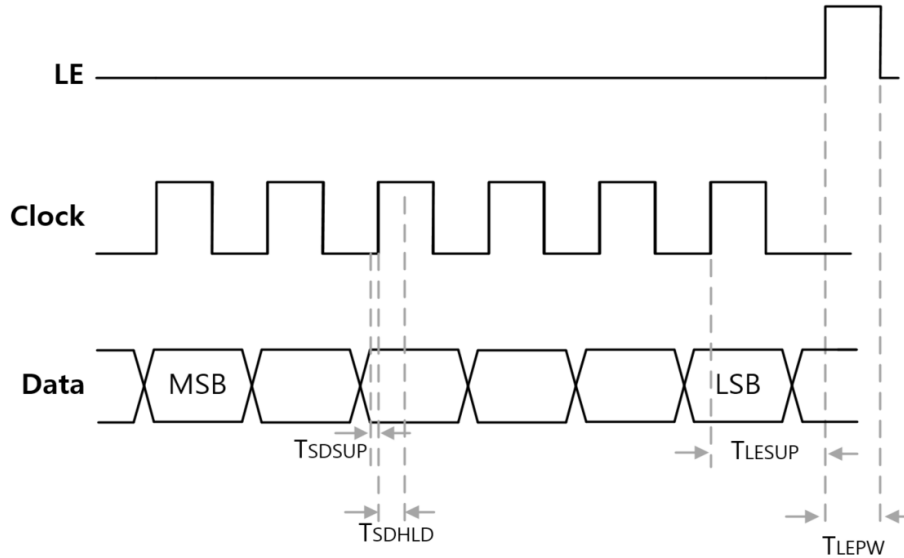
**Table 5. Serial Attenuation word Truth Table<sup>1</sup>**

Attenuation Word						Attenuation State
C16	C8	C4	C2	C1	C0.5	
0	0	0	0	0	0	Reference Loss
0	0	0	0	0	1	0.5 dB
0	0	0	0	1	0	1 dB
0	0	0	1	0	0	2 dB
0	0	1	0	0	0	4 dB
0	1	0	0	0	0	8 dB
1	0	0	0	0	0	16 dB
1	1	1	1	1	1	31.5 dB

<sup>1</sup> Not all 64 possible combinations of C0.5–C16 are shown in table.

**Figure 3. 6-Bit Attenuator Serial Programming Register Map**



**Figure 4. Serial Interface Timing Diagram**

**Table 6. Serial Interface AC Characteristics**

VDD= 5.0V with DSA only,  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ , unless otherwise specified

Symbol	Parameter	Min	Max	Unit
F <sub>CLK</sub>	Serial data clock frequency <sup>1</sup>		10	MHz
T <sub>CLKH</sub>	Serial clock HIGH time	30		ns
T <sub>CLKL</sub>	Serial clock LOW time	30		ns
T <sub>LESUP</sub>	LE set-up time after last clock rising edge	10		ns
T <sub>LEPW</sub>	LE minimum pulse width	30		ns
T <sub>SDSUP</sub>	Serial data setup time before rising edge	10		ns
T <sub>SDHLD</sub>	Serial data hold time after clock rising edge	10		ns

<sup>1</sup> F<sub>CLK</sub> is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify F<sub>CLK</sub> specification

Figure 5. Pin Configuration

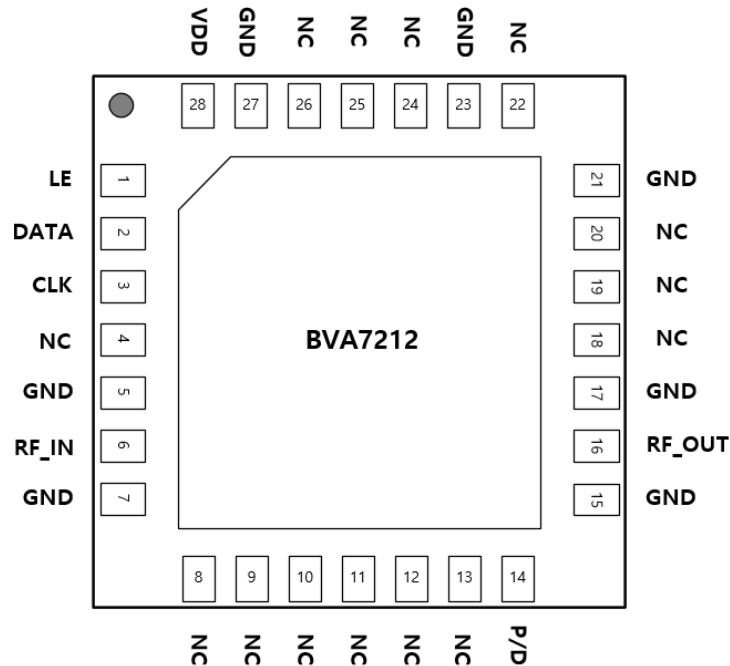


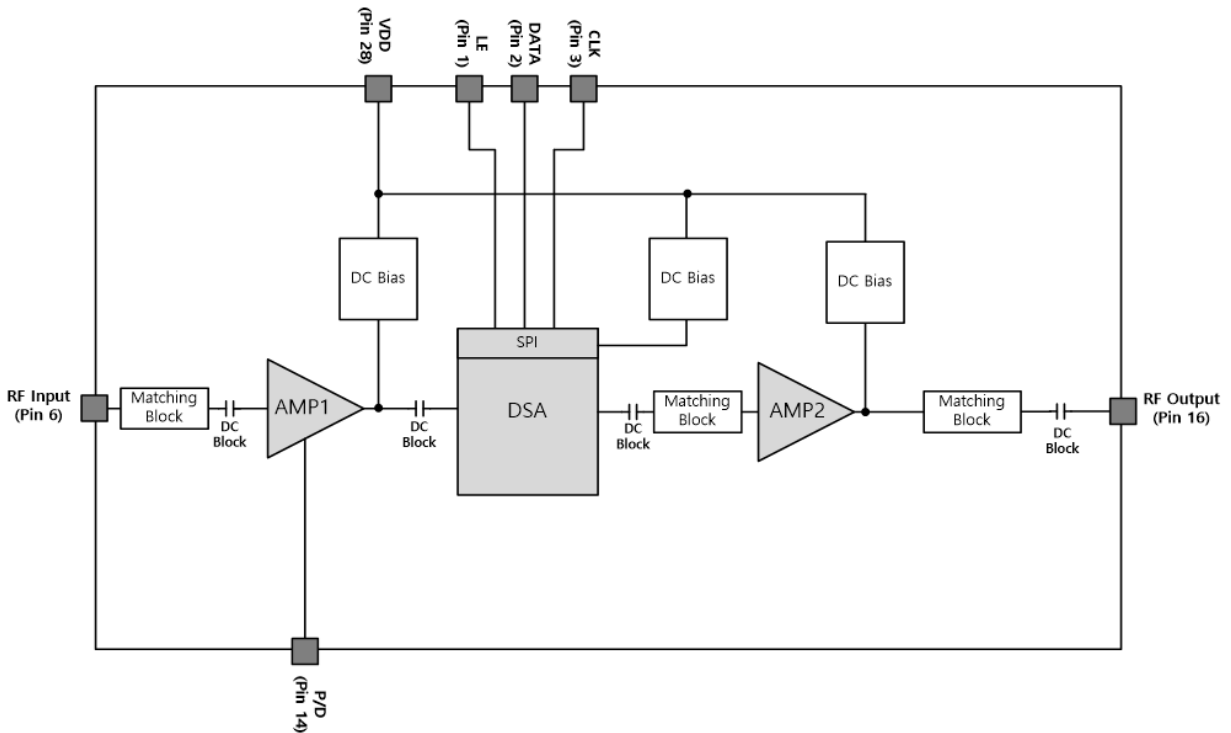
Table 7. Pin Description

Pin	Pin name	Description
5,7,15,17,21,23,27	GND	RF/DC Ground
1	LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial Data Input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial Clock Input.
6	RF_IN	RF input, matched to 50 ohm. Internally DC blocked.
14	P/D	VDD Power Down control Input. With Logic High(1.17 to 5V), Amplifier is Disabled. With Logic Low (0 to 0.63V), Amplifier is Enabled.
16	RF_OUT	RF output, matched to 50 ohm. Internally DC blocked.
28	VDD	SPI and DSA DC supply. This pin is connected to bypass capacitor internally.
4,8-13,18-20,22,24-26	NC	Doesn't matter how these pins are NC (No Connection) or recommend connect to ground.
Exposed Pad	GND	RF/DC Ground

**Figure 6. Internal Function Block Diagram**

The BVA7212 is integrated two gain blocks (AMP1, AMP2) and one digital step attenuator (DSA). Additionally, the BVA7212 includes an internal bias circuits and RF Matching to improve the RF performances at 1.4GHz - 2.3GHz.

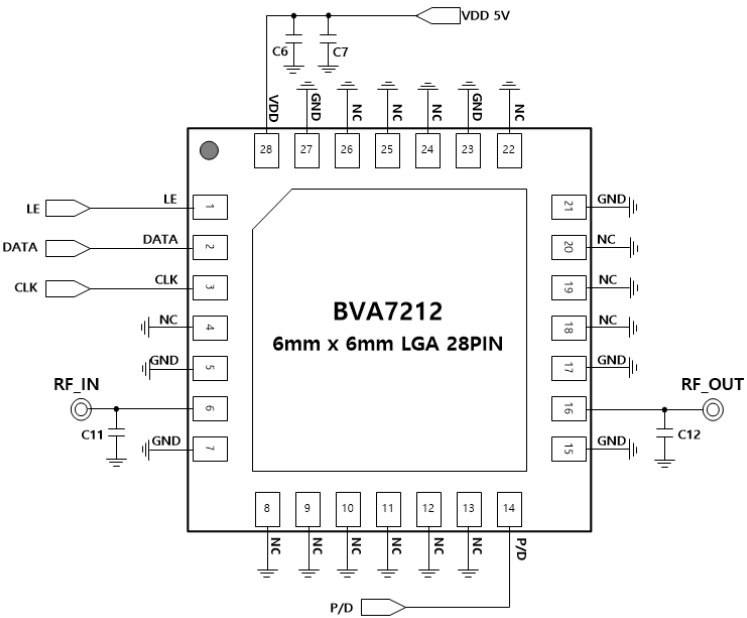
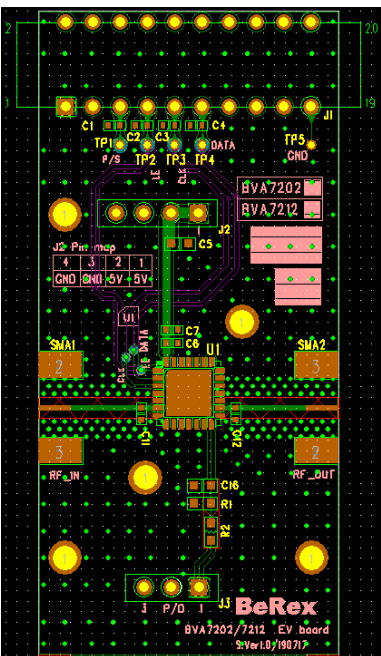
The block diagram of BVA7212 is shown below.



#### Typical RF Performance - BVA7212 EVK - PCB

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted.

**Table 8. Application Circuit**

Schematic Diagram	BOM			Remark
	Ref	Size	Value	
	C6	0402	1 nF	
	C7	0402	100 nF	
	C11	0402	DNI	
	C12	0402	DNI	
	NOTE			
	1. J1 Information			
	- Pin 5 : Not used. P/S (TP1)			
	- Pin 7 : LE (TP2)			
	- Pin 9 : CLK (TP3)			
	- Pin 11 : DATA (TP4)			
	- Pin 19 : GND (TP5)			
	2. J2 Information			
	- Pin 1, 2 : VDD pin			
	- Pin 3,4 : GND			
3. J3 Information				
- Pin 1 : P/D pin				
- Pin 2, 3 : GND				
- Pin 1 Logic High AMP1 Disabled.				
- Pin 1 Logic Low AMP1 Enabled.				



**Typical RF Performance - BVA7212 EVK**

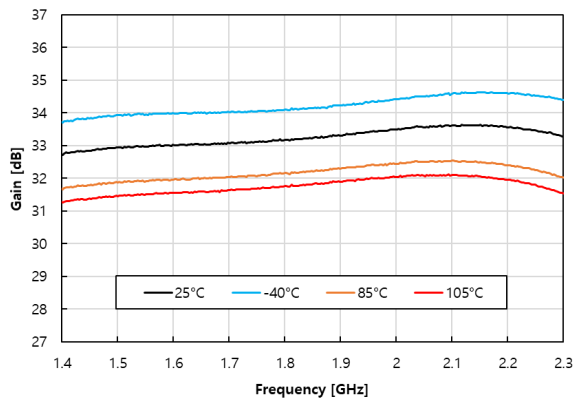
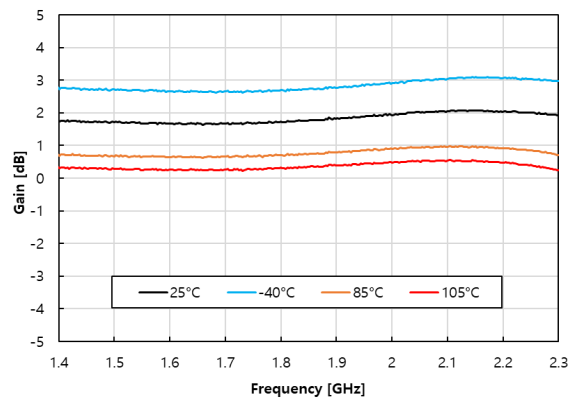
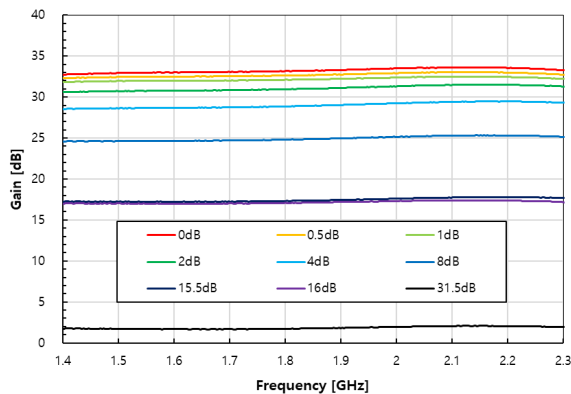
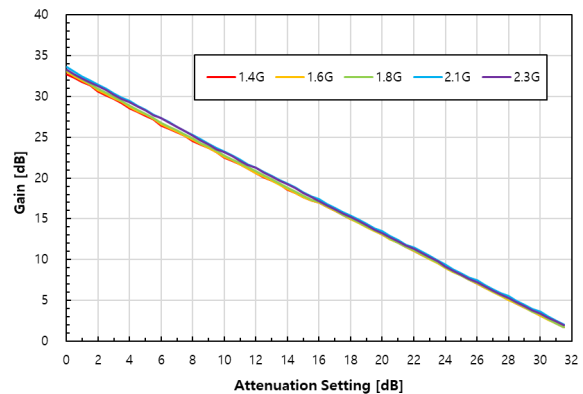
Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

**Table 9. Typical Performance by Temperature<sup>2</sup>: 1.8GHz**

Parameter	Typical Values				Units
	-40	25	85	105	
Temperature	-40	25	85	105	°C
VDD	5	5	5	5	Vdc
Current	175	180	185	183	mA
Gain	34.1	33.2	32.2	31.6	dB
S11	-14.4	-15.3	-16.2	-16.6	dB
S22	-11.6	-12.6	-13.8	-14.3	dB
OIP3 <sup>1</sup>	38.3	40.5	40.3	39.3	dBm
OP1dB	23.9	23.6	23.3	23.2	dBm
Noise Figure	2.7	3.33	3.92	4.02	dB

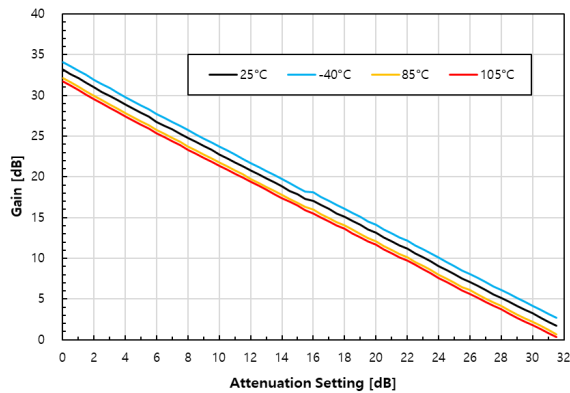
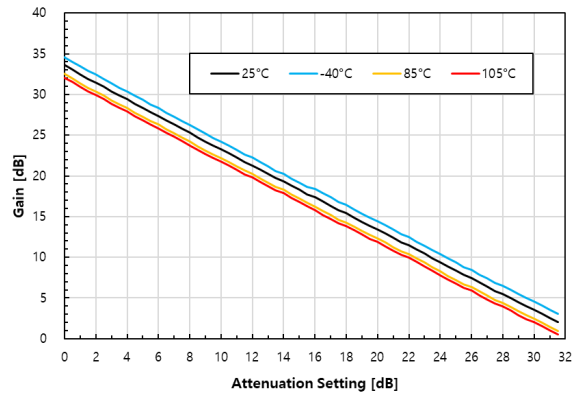
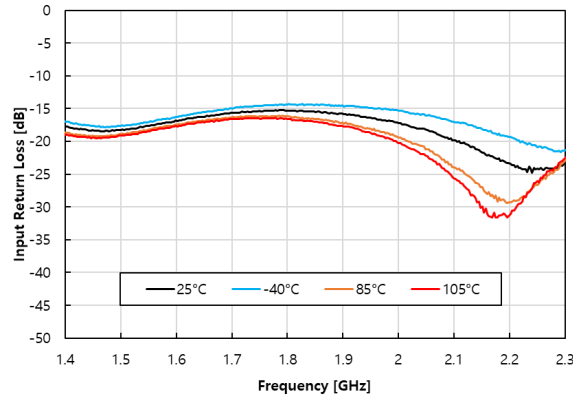
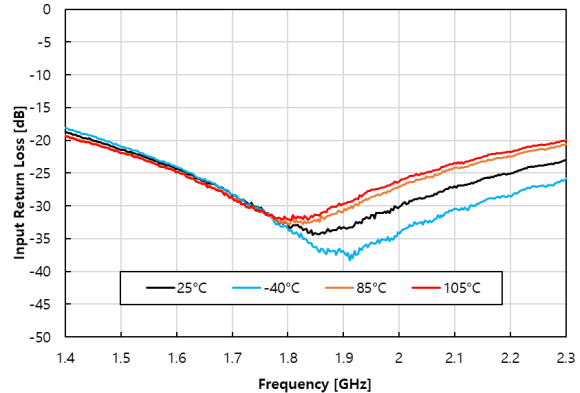
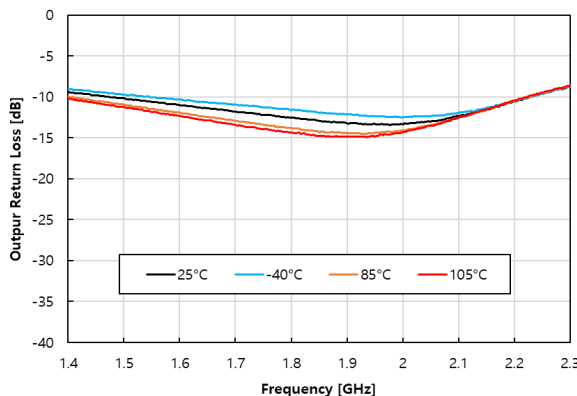
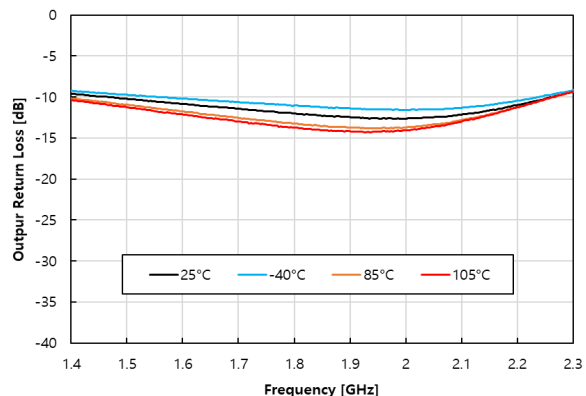
<sup>1</sup> OIP3 measured with two tones at an output of 7dBm per tone separated by 1MHz.

<sup>2</sup> Above test parameters are measured at Max Gain State (ATT=0dB)

**Figure 7. Gain**  
: Max Gain, Temp.

**Figure 8. Gain**  
: Min Gain, Temp.

**Figure 9. Gain**  
: Attenuation Setting

**Figure 10. Gain**  
: Frequency, Attenuation Setting


**Typical RF Performance - BVA7212 EVK**

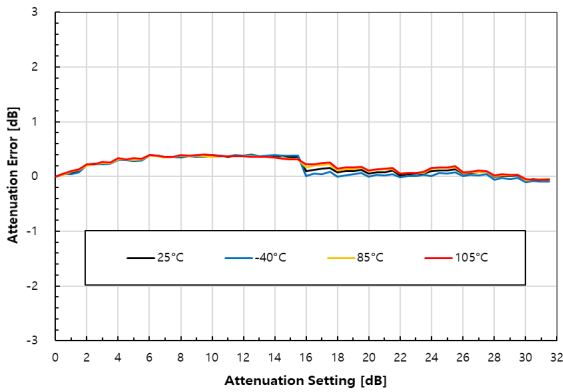
Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

**Figure 11. Gain**  
 : 1.8GHz, Attenuation Setting, Temp.

**Figure 12. Gain**  
 : 2.1GHz, Attenuation Setting, Temp.

**Figure 13. Input Return Loss**  
 : Max Gain, Temp.

**Figure 14. Input Return Loss**

**Figure 15. Output Return Loss**  
 : Max Gain, Temp.

**Figure 16. Output Return Loss**  
 : Min Gain, Temp.


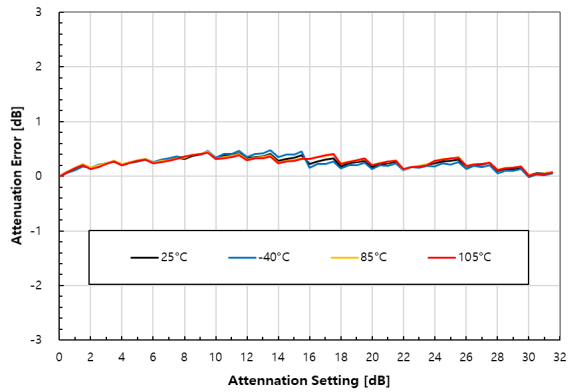
### Typical RF Performance - BVA7212 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

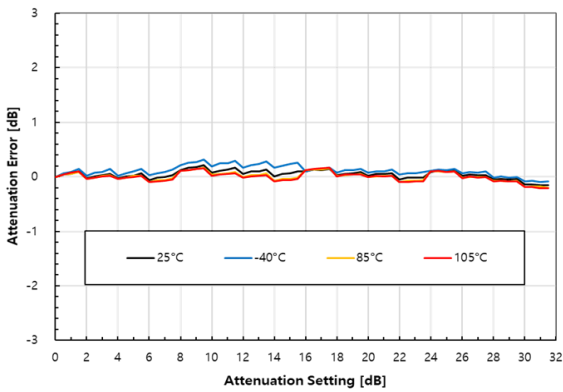
**Figure 17. Attenuation Error**  
: 1.8GHz, Temp.



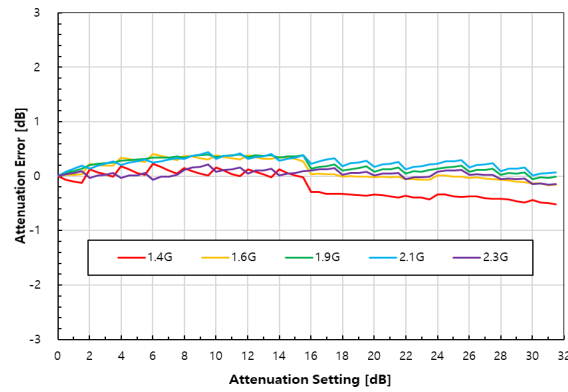
**Figure 18. Attenuation Error**  
: 2.1GHz, Temp.



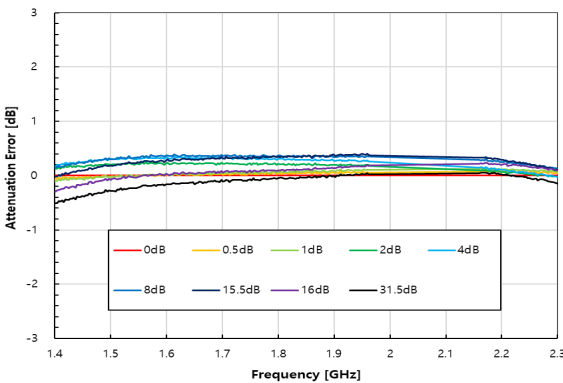
**Figure 19. Attenuation Error**  
: 2.3GHz, Temp.



**Figure 20. Attenuation Error**



**Figure 21. Attenuation Error**  
: Attenuation Setting

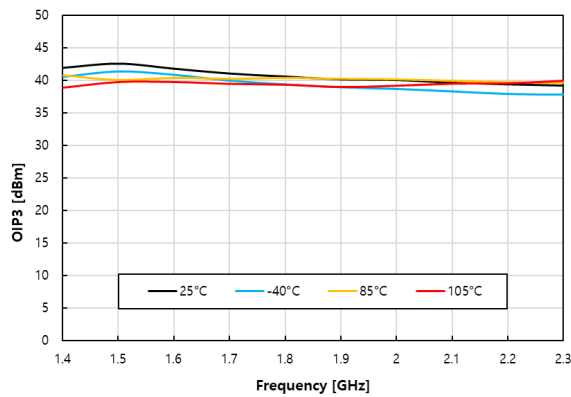


### Typical RF Performance - BVA7212 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

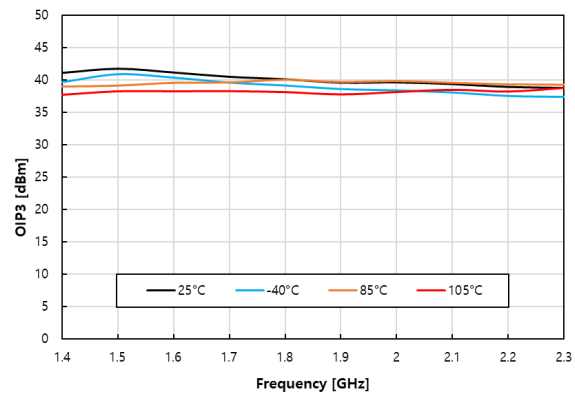
**Figure 22. OIP3**

: ATT=0dB, Temp, Output=7dBm/tone, 1MHz interval



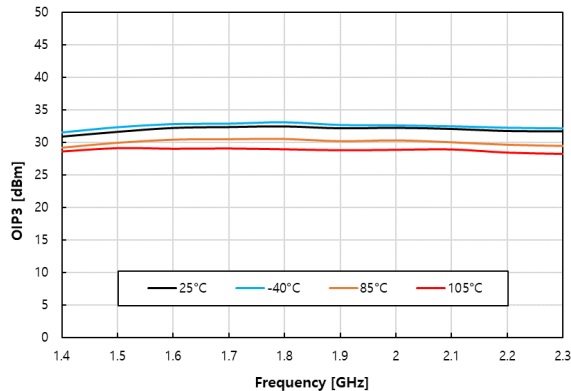
**Figure 23. OIP3**

: ATT=6dB, Temp, Output=7dBm/tone, 1MHz interval



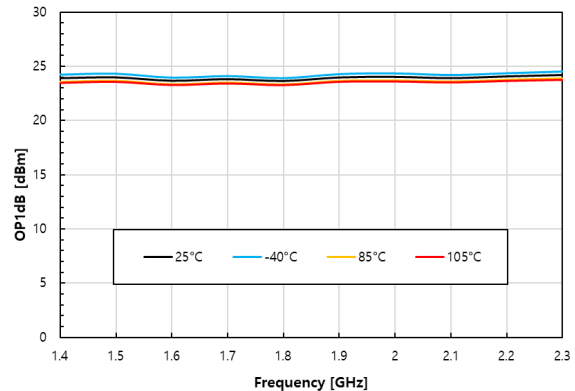
**Figure 24. OIP3**

: ATT=20dB, Temp, Input=-20dBm/tone, 1MHz interval



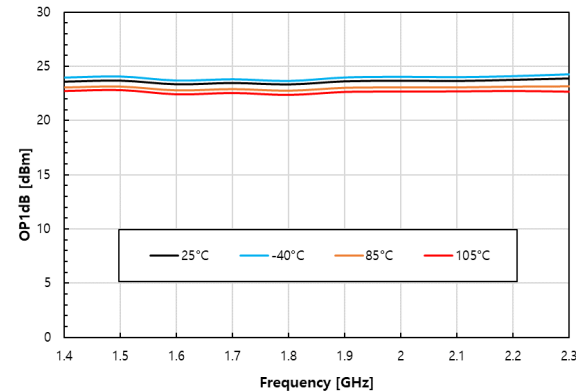
**Figure 25. OP1dB**

: ATT=0dB (Max Gain), Temp.



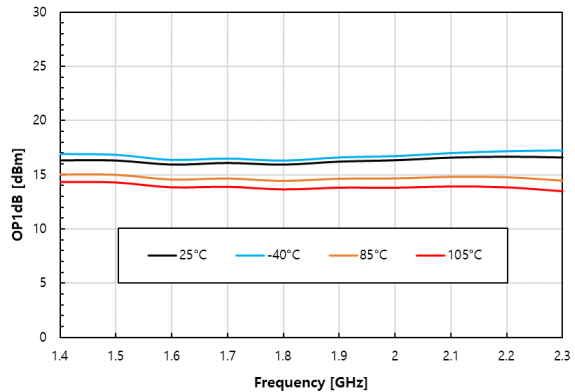
**Figure 26. OP1dB**

: ATT=10dB, Temp.



**Figure 27. OP1dB**

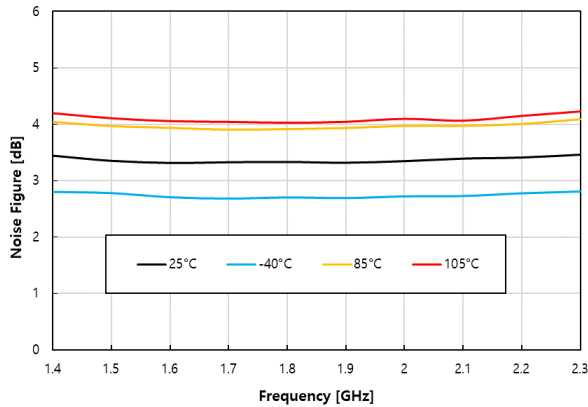
: ATT=20dB, Temp.



### Typical RF Performance - BVA7212 EVK

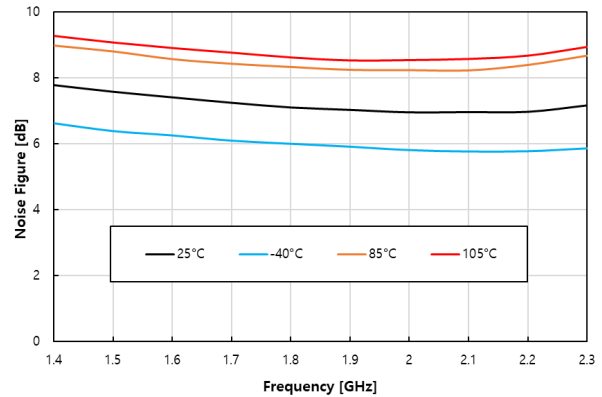
Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

**Figure 28. NF**



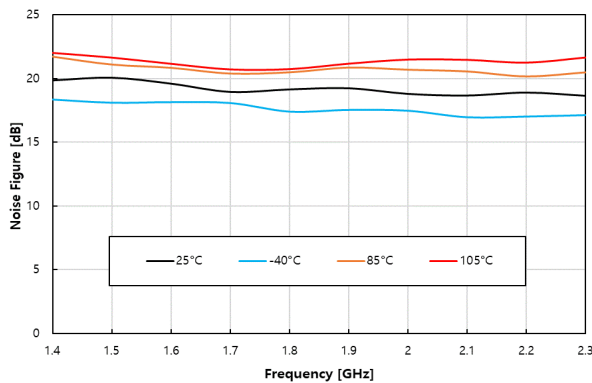
**Figure 29. NF**

: ATT=15dB, Temp.



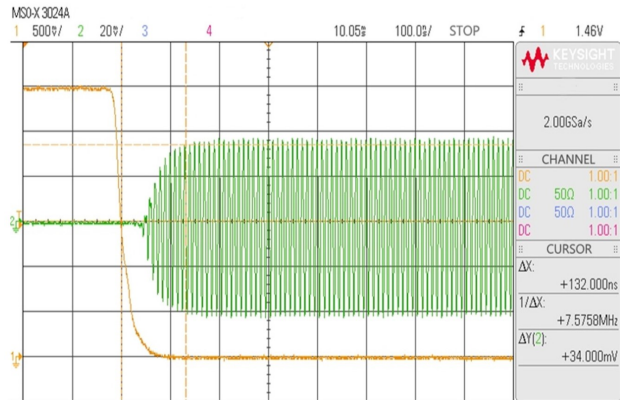
**Figure 30. NF**

: ATT=29.5dB, Temp.



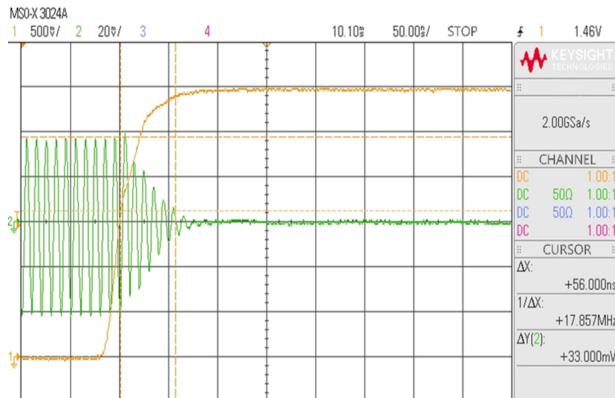
**Figure 31. Power On/Off Time**

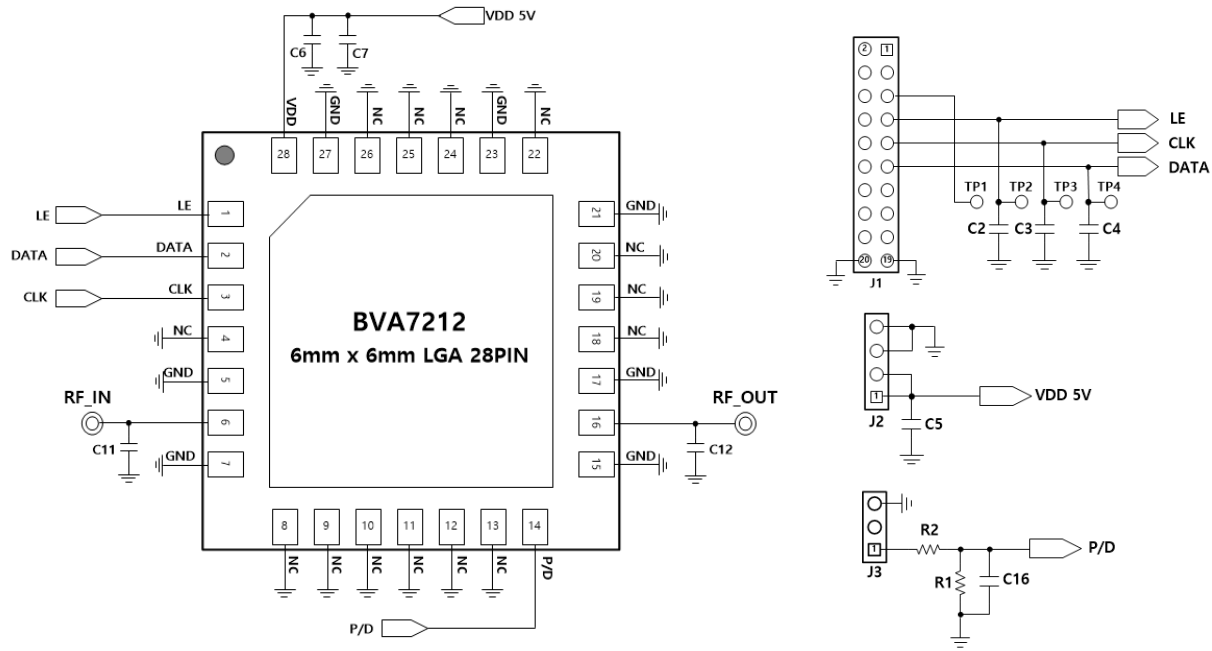
: Rising Time (Control 50% to RF 90%)



**Figure 32. Power On/Off Time**

: Falling Time (Control 50% to RF 10%)



**Figure 33. Evaluation Board Schematic**

**Table 10. Bill of material**

No.	Ref. Number	Value	Description	Remark
1	R2	0 ohm	Resistor, 0603, Chip, 5%	Walsin
2	C6	1000 pF	1 nF $\pm 5\%$ , 16V, X7R Ceramic Capacitor (0402)	Murata
3	C7	100 nF	100 nF $\pm 10\%$ , 16V, X7R Ceramic Capacitor (0402)	Murata
4	SMA1	SMA	SMA(F) Connector, PCB Mount, PSF-S01-007	Gigalane
5	SMA2	SMA	SMA(F) Connector, PCB Mount, PSF-S01-007	Gigalane
6	J1	20pin	Receptacle Connector, 5-532955-3, Female, RT/A Dual	AMP Connectors
7	J2	4pin	2.54mm Breakaway Male Header, Straight, Black	
8	J3	3pin	2.54mm Breakaway Male Header, Straight, Black	
9	R1,C1,C2,C3,C4, C5,C11,C12,C16	DNI		

RF Input was matched by Inductor internally. So that it needs DC Blocking Capacitors when DC voltage is presented at RF input port.

Figure 34. Evaluation Board Layout

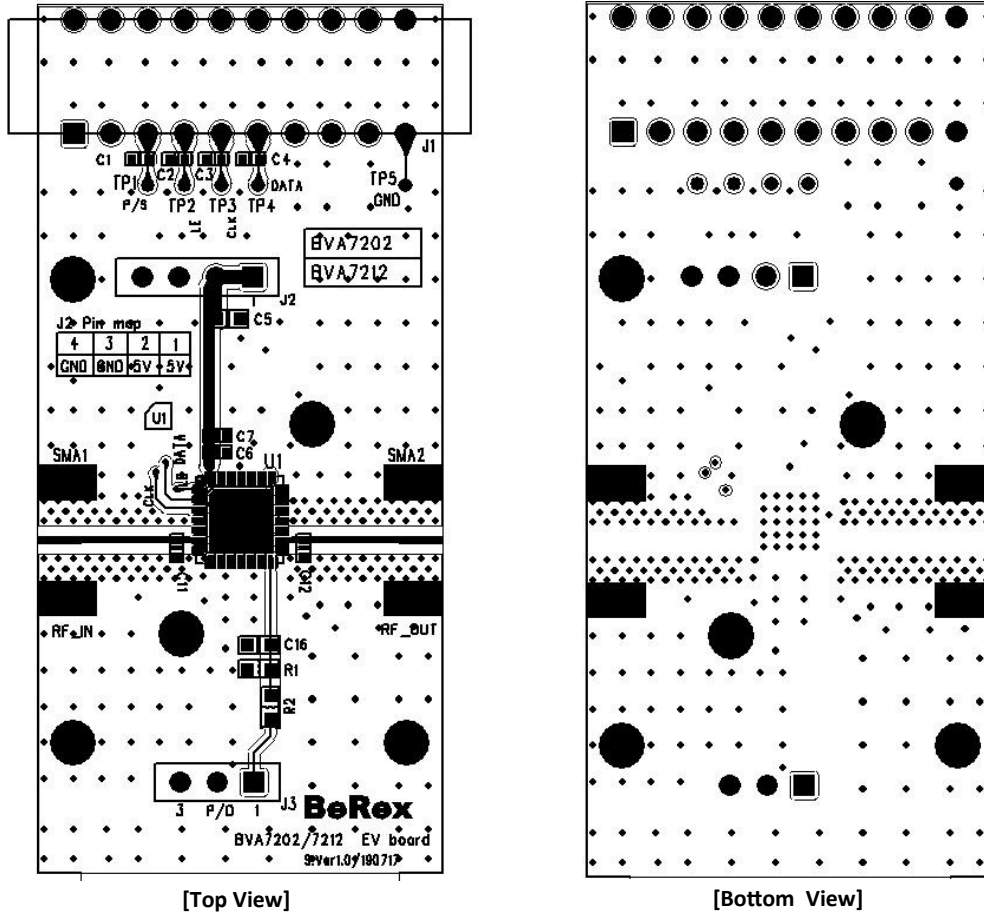
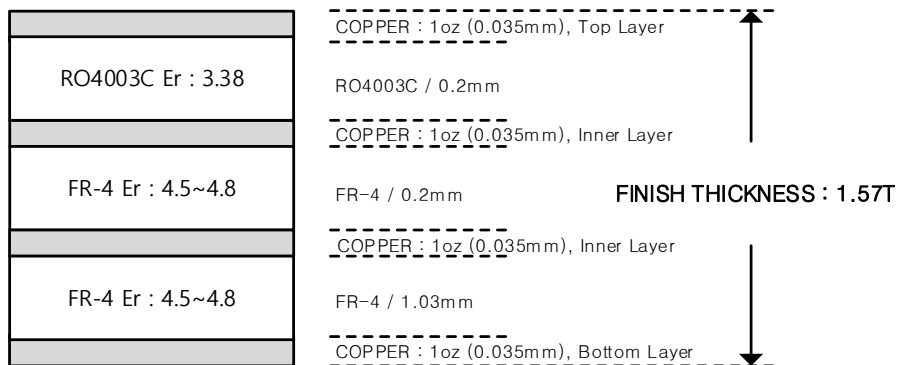
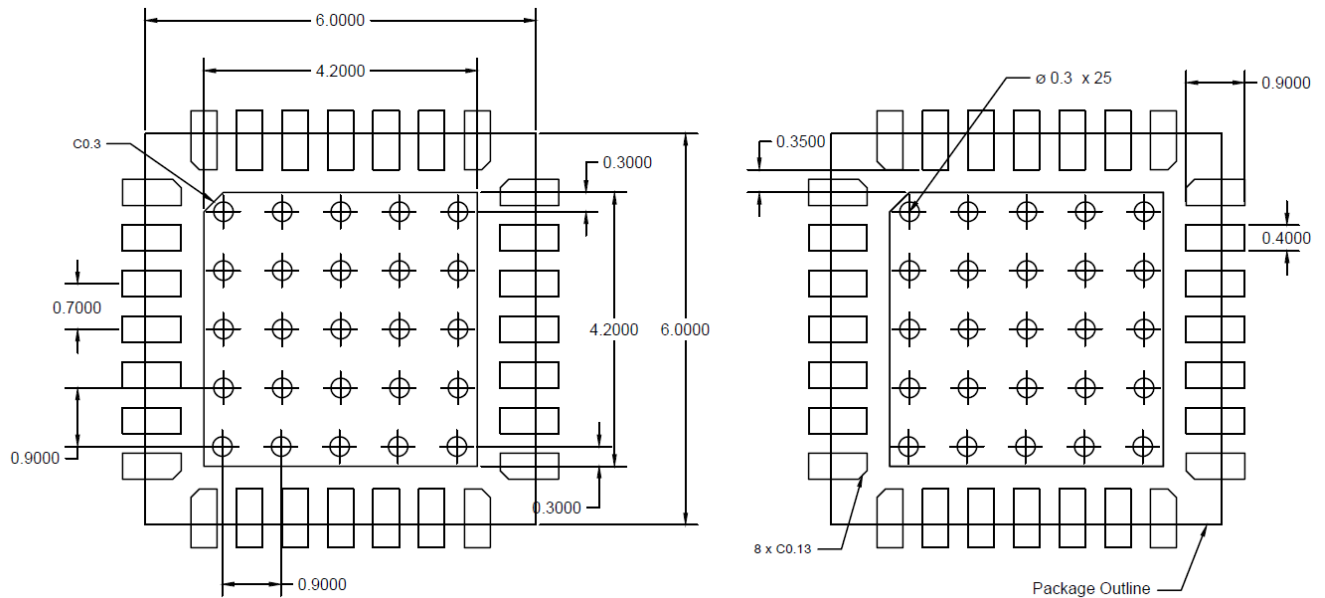
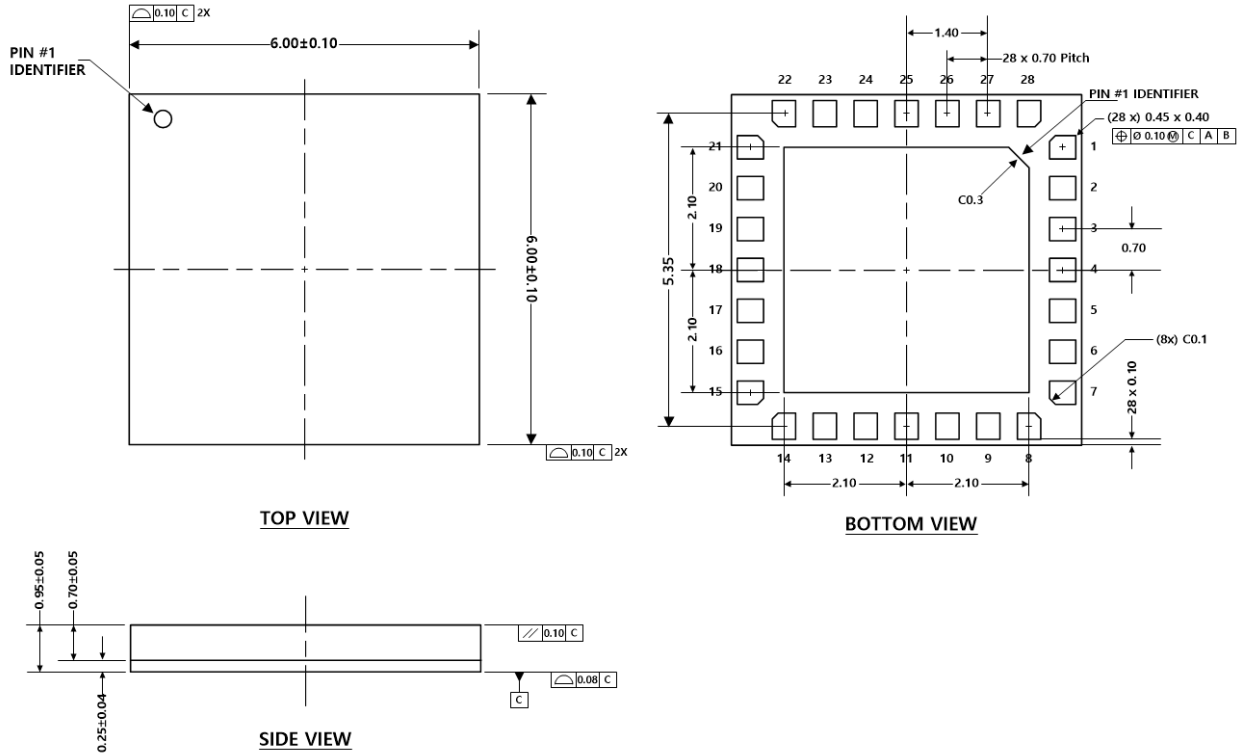


Figure 35. Evaluation Board PCB Layer Information

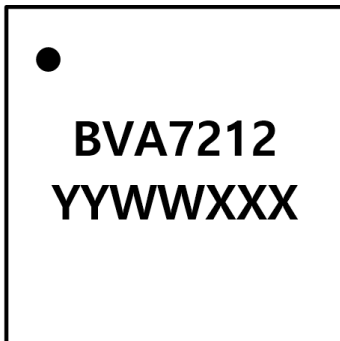


**Figure 36. Suggested PCB Land Pattern and PAD Layout**


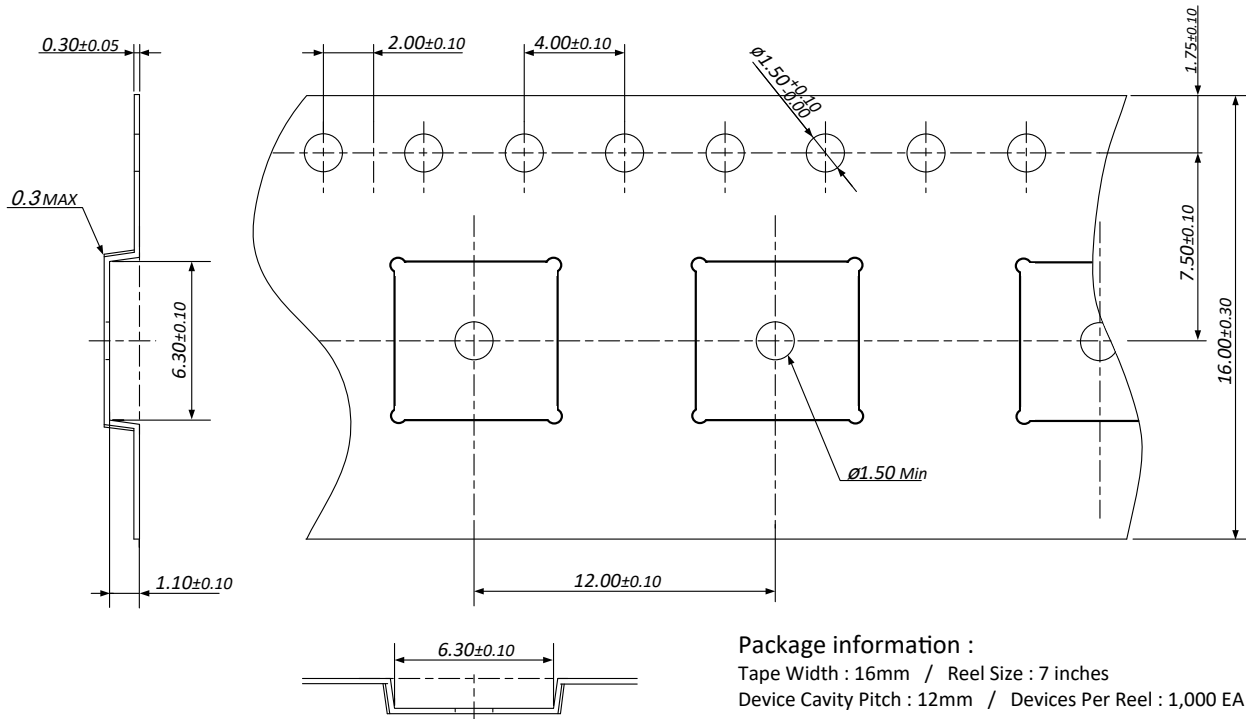


**Figure 37. Package Outline Dimension**

**Notes**

1. All dimensions are in millimeters. Angles are in degrees
2. Dimensions and tolerance conform with ASME Y14.5M-1994.

**Figure 38. Package Marking Information**


YY = Year  
 WW = Working Week  
 XXX = Wafer Lot Number

**Figure 39. Tape and Reel**


**Lead Plating Finish**

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

**MSL / ESD Rating**

ESD Rating : Class 1C  
Value : 1000V  
Test : Human Body Model (HBM)  
Standard : JEDEC Standard JS-001-2017

ESD Rating : Class C5  
Value : 1000V  
Test : Charged Device Model (CDM)  
Standard : JEDEC Standard JESD22-C101F

MSL Rating : MSL3  
Standard : JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling the device.

**RoHS2 Compliance**

BVA7212 is compliant with 2011/65/EU RoHS2 directive. (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic equipment.)

**NATO GAGE Code :**

2	N	9	6	F
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